A Temperature-Insensitive Self-Recharging Circuitry Used in DRAMs

Chua-Chin Wang, Yih-Long Tseng, Chih-Chiang Chiu

Abstract— **This paper presents a practical self-recharging circuitry for DRAMs. The proposed self-recharging circuitry not only reduces the standby power by monitoring the voltage drop caused by the data loss of a memory cell, but also adjusts the recharging period of the memory cell which is resulted from leakage currents. The proposed design is insensitive to temperature variations. A 1-Kb DRAM using our design is fabritcated by TSMC 0.35 μm 1P4M CMOS process. The physical measurement of the proposed design on silicon verifies the correctness of the proposed circuitry.**

Index Terms— **adaptive self-recharging circuitry, DRAM, self-recharge**

I. INTRODUCTION

The trend toward portable and small digital equipments or systems is rapidly booming [1]. Hence, the reduction of data retention power of DRAMs is one of the major targets in memory designs [2], [3]. Self-recharging methodology perhaps is the most widely used scheme to reduce the data retention power. However, extending the recharging period which has been considered an effective way to reduce the data retention power can not catch up the evolution of the number of memory cells which is increased four times every generation. It is very difficult to extend the data retention time by four times every generation, since the cell size and the supply voltage are scaled in deep sub-micron technology. Besides, prior self-recharging methods are either mode selection schemes [2], [4], [5] or by pseudo-SRAM schemes [3], [6]. They are still vulnerable to the temperature variations and unable to adjust the recharging period accordingly. In this paper, we present a novel self-recharging design for DRAMs by monitoring the voltage drop of the data loss in the memory cell. As soon as the voltage drop reaches the amount of a threshold voltage, a recharging signal is triggered to boost the data back to its original voltage level. Hence, the recharging period will not depends on any mode selection. When the temperature varies, the recharging period also changes accordingly.

II. ADAPTIVE SELF-RECHARGING CIRCUITRY(ASC)

Most of the prior self-recharging designs for DRAMs were focused on the mode selections in which certain mechanisms monitor a few parameters and then initiate one of several oscillators with pre-determined recharging periods. However, this scheme is very prone to the temperature variations. The reason is given as follows. The leakage current I_{leak} of a MOS device can be expressed as:

$$I_{leak} = \frac{W_{eff}}{W_o} \cdot I_o \cdot 10^{(V_{GS}-V_{th})/S} \tag{1}$$

where W_o and I_o are reference channel width and current level to determine the threshold voltage of the MOS device. W_{eff} is the effective channel width of the transistor. S is the swing parameter.

Referring to BSIM3 MOS model, the threshold voltage V_{th} of a MOS device can be expressed as:

$$\begin{aligned} V_{th}(T_{device}) &= V_{th}(T_{NOM}) + [KT1 + \frac{KT1L}{L_{eff}} \\ &+ KT2 \cdot V_{BS}] \cdot (\frac{T_{device}}{T_{NOM}} - 1) \end{aligned} \tag{2}$$

where T_{NOM} is the room temperature, and T_{device} is the device temperature. $KT1$ is the main temperature coefficient of the threshold voltage, and $KT1 \leq 0$. $KT1L$ is used to improve fitting the dependence on the channel length, and $KT1L$ is default to be 0. $KT2$ is used to improve fitting the dependence on bulk bias's effects. V_{BS} is the bulk to substrate voltage. L_{eff} is the effective channel length of the MOS device. If $T_{device} > T_{NOM}$, $KT1 + \frac{KT1L}{L_{eff}} + KT2 \cdot V_{BS}$ is negative. When T_{device} rises, V_{th} decreases. So does I_{leak}. A short recharging period, then, is required. In order to keep correct data in all the DRAM cells, the recharging period must be kept with the shortest period given the highest operation temperature. The redundant recharging cycles in a lower temperature condition is nothing but power wasting. A self-recharging circuitry adapting with temperature variations can resolve this problem.

A. Self-recharging datapath

A simple thought to initiate a recharging cycle is to monitor a specific parameter which is supposed to be varied with the temperature in order to avoid those drawbacks introduced by the prior works. Another consideration is that the data loss must be avoided, either. Hence, an effective way to initiate a recharging cycle is to monitor the voltage of the data in the memory cells. As soon as it drops by a V_{th}, a threshold voltage, the recharging cycle is triggered to recharge the cell to retain the data. Referring to Fig. 1, the datapath of the initiation of a self-recharging cycle consists of a memory cell, a voltage comparator, and a control signal generator (CSG). The ENABLE signal is to activate the control signal generator

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to start recharging cycles. The inputs to the comparator are the output of the memory cell and one reference voltage, V_{ref}=VDD-V_{th}. The output of the CSG is fed back to restore the voltage of the memory cell such that the data loss is compensated. The key point of such a design is that since the V_{th} and $I_{leakage}$ are temperature dependent, the duration for the voltage drop of the memory cell which is determined by the deterioration of V_{th} and the leakage current also depends on temperature variations. This leads to that the entire self-recharging design is adaptive. Table I shows the MAX and MIN V_{th} in TSMC 0.35 μm CMOS process given in different temperatures.

B. Circuitry of the datapath

Memory cell : Referring to Fig. 2, the memory cell and the emulated leakage current source are shown. As soon as the RECHARGE is high, P1 and N2 are turned on to recharge the data at gate of N1. If RECHARGE is low, N2 is off. In the meantime, the cascode load of N7, N6, and N5 supplies a tiny current which is roughly tuned to be in the range of the leakage current and the subthreshold current. N3 and N4 consist of a current mirror to mimic the data degradation. The charge at the gate of N1 will be leaked via N3 of which the gate is driven by the current mirror. Assume that $T_{recharge}$ is the duration for the cell to restore its voltage level. Meanwhile, there are a total of n rows in the memory. Thus, the recharging duration for each row becomes $\frac{T_{recharge}}{n}$. Hence, in order to speed up the self-recharging, the N3 and N4 might be added purposely.

Comparator : A voltage comparator, as shown in Fig. 3, is required to monitor the voltage drop of the cell. P31, P32, N31, and N32 provides a voltage reference. When all of these four transistors are saturated, the voltage at node A is V_{ref} = VDD-V_{th}. Referring to Eqn. (2), when the temperature rises, the threshold voltage goes down, and the V_{ref} goes up. The higher V_{ref} makes DET rise earlier, and speeds up the recharging cycles. P33, P34, N33, N34, and N35 consist of a differential amplifier of which inputs are the voltages of the cell and node A. As soon as the cell voltage drops to V_{ref}, node B is pulled down to turn on P35 such that a high strobe is generated at DET given that N36 is properly biased. The precision of the comparator in different temperatures is shown in Table II.

CSG : Referring to Fig. 4, the schematic of the CSG is illustrated. The external ENABLE signal is detected by the rising edge detector (RED) to validate the DET signal fed by the comparator. NAND2 and NAND3 consists of a SR latch which extends the length of the valid strobe by the DELAY module. A voltage level shifter comprising P41, P42, N41, N42, and INV2 to boost the OUT to be VDD+V_{th} which is fed to the RECHARGE in Fig. 2. Notably, the power supply of the level shifter is VDD+V_{th} instead of VDD owing to that the recharging path is via an NMOS, N2, to the data cell, N1. Thus, the voltage at RECHARGE must be VDD+V_{th} to restore the gate of N1 back to VDD. The RED module and the DELAY module are shown in Fig. 5 and 6, respectively.

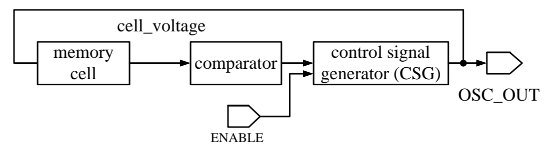

Fig. 1. Datapath of the proposed design

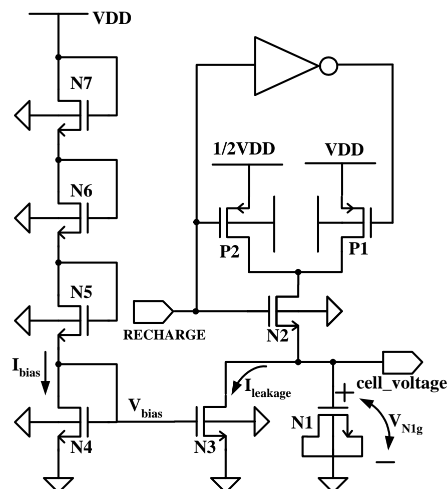

Fig. 2. Memory cell

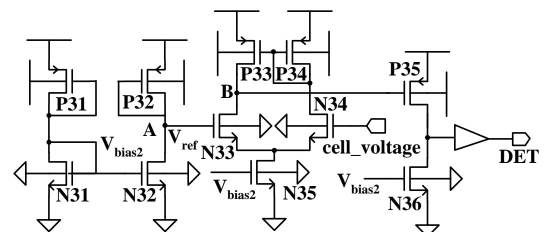

Fig. 3. Comparator

III. Chip Implementation and Measurements

In order to verify the robustness of the proposed self-recharging design, we carry out the implementation of a 1-Kb DRAM by using TSMC 0.35μm 1P4M CMOS process. We have simulated every transistor model, including FF, TT, and SS, at a variety of temperature, e.g., 0^oC, 25^oC, 70^oC, 85^oC, and 110^oC, to attain the recharging performance. Although Table III only shows the comparison of recharging period of TT-modeled MOS transistors, the performance of the other models are very muck alike. Fig. 7 is the graph showing the leakage current and the voltage of the memory cell at different temperatures. The DRAM is 1K bits which needs $2^{\frac{12}{2}} = 32$ rows. Assume the VDD is 3.3V and the threshold voltage is 1.2V. It implies that the cell needs to be recharged when it drops to 3.3 - 1.2 = 2.1V. According to Fig. 7, we are then aware of the following maximum recharging periods.

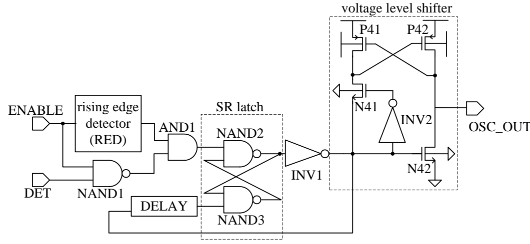

Fig. 4. Schematic of CSG

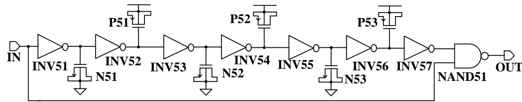

Fig. 5. rising edge detector(RED)

$$0^o \rightarrow T_{recharge} = (7.71ms/32)/4 = 60.24\mu s$$

$$85^o \rightarrow T_{recharge} = (7.06ms/32)/4 = 55.16\mu s$$

$$100^o \rightarrow T_{recharge} = (5.01ms/32)/4 = 39.14\mu s$$

$$110^o \rightarrow T_{recharge} = (3.01ms/32)/4 = 23.52\mu s$$

The extra divided-by-4 in the above equations is to ensure that the recharging will be successfully done by shortening the period. Fig. 8 shows the simulation results of the proposed design. Fig. 9 reveals the voltage and the current at several temperatures. It is obvious that the recharging period is adaptive according to the temperature variations.

Fig. 10 shows the die photo of the overall 1-Kb DRAM with the proposed self-recharging circuitry. Fig. 11 is the waveforms of the recharging oscillator physically measured by HP 54616C OSC at 30^oC, 40^oC, 50^oC, 60^oC. Table IV summarizes the recharging periods given different temperatures. The switching power consumption of the self-recharging circuits ($P_{switching}$) can be simplified as follow equation:

$$P_{switching} = C \cdot V^2 \cdot f \quad (3)$$

where C is the capacitance of the self-recharging circuits, V is the system VDD, and the f is the recharging frequency. In order to keep correct data in DRAM cells, the recharging period must match the requirement of the highest operation temperature. If a fixed recharging period is adopted, the power waste is severe in a lower temperature condition. Referring to Table IV, if the recharging period is fixed to be 465 ns, the $P_{switching}$ wastes 23.77 % power in 30^oC, 12.26% in 40^oC, and 4.12% in 50^oC, respectively. If we use a multi-period recharging scheme similar to [4] and the recharging period is fixed with those at 0^oC, 30^oC, and 60^oC, it is still 12.26% worse than our design in 40^oC and 4.12% in 60^oC.

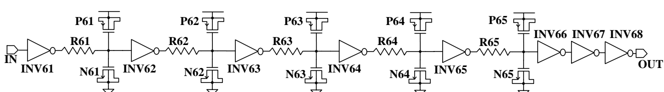

Fig. 6. DELAY module

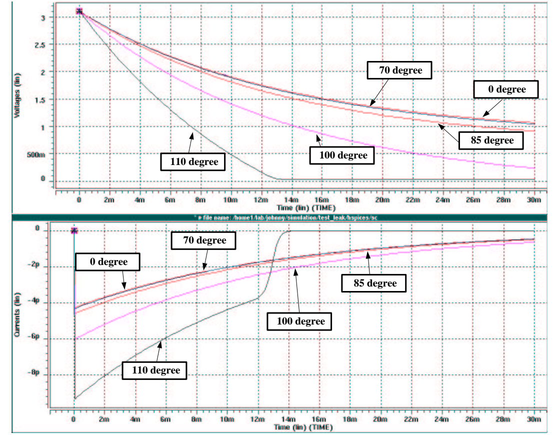

Fig. 7. Voltage and leakage current at the cell_voltage node in Fig. 2

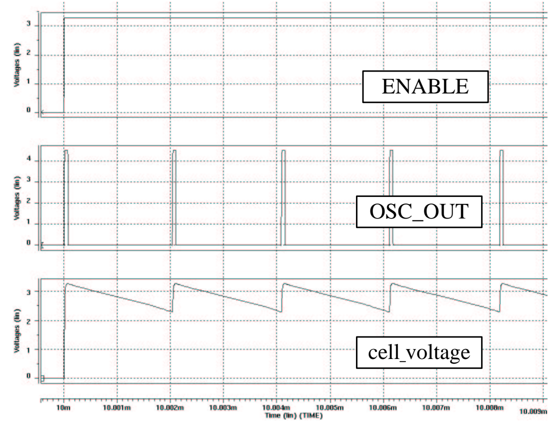

Fig. 8. Simulation results of the proposed design

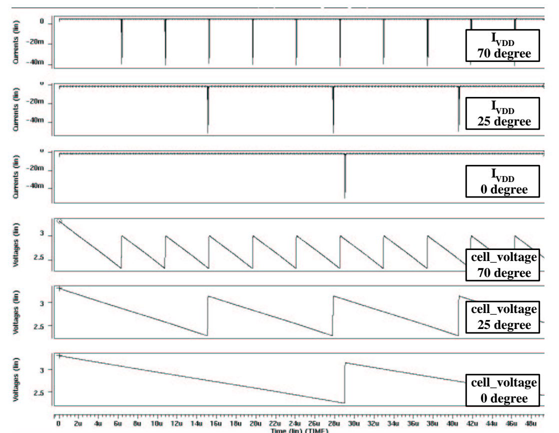

Fig. 9. Current and voltage at different temperatures(I_{VDD}: the current of the VDD of the refresh oscillator)

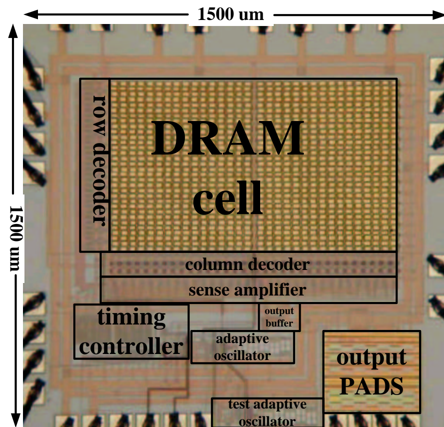

Fig. 10. Die photo of the 1-Kb DRAM design

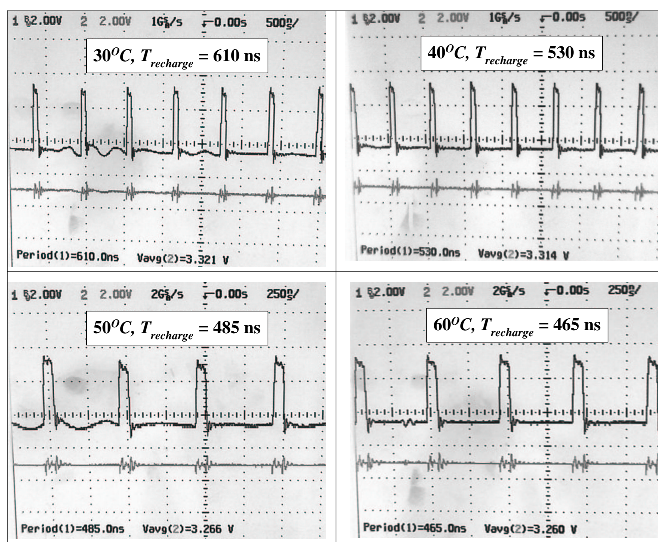

Fig. 11. The waveforms of the refreshing oscillator at different temperatures

IV. Conclusion

A novel self-recharging oscillator design is proposed to be added in DRAMs. The shortcoming of the pre-determined recharging cycles in prior works is eliminated. The proposed design is proved on silicon to be temperature insensitive. On top of these advantages, the power dissipation will also be reduced since the unwanted recharging cycles no longer exist. All of the proposed circuits have been proved by the physical measurement results.

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TABLE I

Max and Min PMOS threshold voltages in different temperatures

	0^oC	25^oC	70^oC	85^oC	110^oC
MAX (Slow model)	0.8086	0.7677	0.6940	0.6695	0.6286
MIN (Fast model)	0.6975	0.6554	0.5796	0.5544	0.5123

TABLE II

Detect precisions (DET: $0 \rightarrow 1$) of the comparator in different temperatures

	cell_voltage	V_{ref}	detection precision
0^oC	$2.42V$	$2.50V$	$0.08V$
25^oC	$2.44V$	$2.53V$	$0.09V$
70^oC	$2.46V$	$2.60V$	$0.14V$
85^oC	$2.47V$	$2.62V$	$0.15V$
110^oC	$2.49V$	$2.65V$	$0.16V$

TABLE III

Simulations of the proposed self-recharging circuitry in the 1-Kb DRAM (MOS model = TT)

	0^oC	25^oC	70^oC	85^oC	110^oC
$T_{recharge}$	$3.03\mu s$	$1.98\mu s$	$1.10\mu s$	$0.92\mu s$	$0.54\mu s$
V_{bias}	$0.583V$	$0.581V$	$0.578V$	$0.577V$	$0.575V$
I_{bias}	$0.434\mu A$	$0.647\mu A$	$1.138\mu A$	$1.302\mu A$	$1.600\mu A$
$I_{leakage}$	$0.602\mu A$	$0.911\mu A$	$1.608\mu A$	$1.868\mu A$	$2.320\mu A$
min. V_{N1_g}	$2.27V$	$2.29V$	$2.31V$	$2.32V$	$2.33V$
max. V_{N1_g}	$3.28V$	$3.27V$	$3.23V$	$3.20V$	$2.97V$

(Note : V_{N1_g} is the gate drive of NMOS N1 in Fig. 2).

TABLE IV

Adaptive self-recharging circuitry (ASC) power saving and physical measurement results of the recharging period in different temperatures

	30^oC	40^oC	50^oC	60^oC
$T_{recharge}$	$610ns$	$530ns$	$485ns$	$465ns$
$ASC\ power saving$	23.77%	12.26%	4.12%	0%