ZigBee 868/915 MHz Modulator/Demodulator for Wireless Personal Area Network

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***Abstract*— This paper presents an architecture as well as circuit implementation of a ZigBee modulator/demodulator in the transceiver for personal area network, which is compliant with the physical layer of IEEE standard 802.15.4. A test prototype has been designed and fabricated using 0.18-μm single-poly six-metal CMOS process with core area of 0.16 mm^2. The measurement results show that packet error rate (PER) is less than 1% given SNR = 5 dB. The total power consumption is merely 251 μW at a 2.4 MHz system clock.**

***Index Terms*— ZigBee, matched filter, direct sequence spread spectrum, low power, wireless network.**

I. Introduction

ZIGBEE is a novel wireless technique based on the IEEE 802.15.4 wireless personal area network (WPAN) standard [1], which primarily aims at a low data rate, low cost, and low power wireless communication. The physical (PHY) layer and media access control (MAC) layer of ZigBee follow [1], and the application layer and the security layer are specified by ZigBee Alliance [2]. The major applications of ZigBee are focused on sensor and automatic control, such as personal medical assistance, industrial control, home automation [3], remote control and monitoring. It is particularly suitable for biotelemetry applications because of low power consumption, e.g., the personal medical monitoring device for senior citizens. Rather than the traditional wired monitoring equipment, the biotelemetry techniques, e.g., [4], [5], [6], and [7], allow electrical isolation from data processing device and power lines [8].

Fig. 1 shows the application of using ZigBee transceivers in the personal medical scenario. The ZigBee transceiver can be installed in the personal medical assistance device carried by the subject. These devices monitor the subject's physiological parameters and transmit these data to an indoor base station for further processing. Once the emergency is detected, the computer can alarms the medical emergency network immediately.

According to the transmitting frequency, the physical layer of the ZigBee can be distinguished into 2.4 GHz mode and 868/915 MHz mode (868 MHz for North American and 915 MHz for Europe). The data rate and the modulation scheme for these two modes are different. Owing to the demand of low data rate and simple modulation scheme, the ZigBee using 868/915 MHz band possesses the edge of the cost over the ZigBee using 2.4 GHz band. This paper presents a ZigBee modulator/demodulator in the transceiver for Personal Medical Assistance using 868/915 MHz band. The specifications of data rate and frequency band are summarized in Table I [11]. ZigBee utilizes the direct sequence spread spectrum (DSSS) technique, where every bit is spread as 15 chips. Hence, the chip rate is fifteen times of the bit rate.

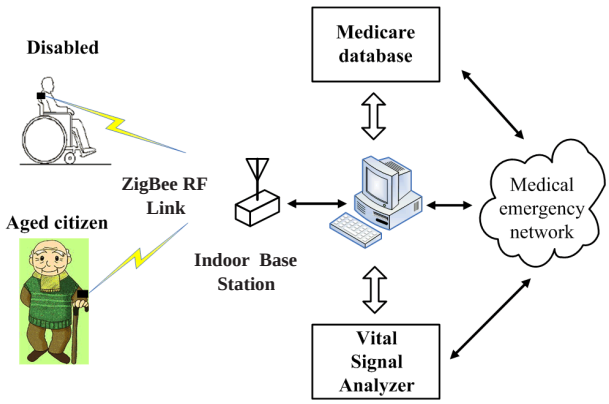

Fig. 1. Application of using ZigBee in personal medical assistance

TABLE I

Specification of data rate and frequency band

Freq. Band (MHz)	Bit Rate (Kb/s)	Chip Rate (Kchip/s)	Modulation
868/915 MHz	20/40	300/600	BPSK

II. ZigBee TRANSCEIVER FOR 868/915 MHZ BAND

Fig. 2 depicts the structure of the ZigBee physical layer protocol data unit (PPDU) packet. The preamble field, which contains 32 bits "0", is for the packet detection and the synchronization in the receiver. The Start of frame delimiter (SFD) field denotes the start of the packet data. The frame length field indicates the number of octets of the physical layer service data unit (PSDU). The PSDU conveys the payload of the packet.

Fig. 3 shows the detailed block diagram of the ZigBee transceiver. The RF signal is down-converted to baseband by the RF receiver (Rx) and quantized by the analog-to-digital converters (ADC). These digital signals are sent to

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Octets : 4	1	1		variable
Preamble	Start of frame delimiter	Frame length (7 bits)	Reserved (1 bit)	PSDU
Synchronization header		PHY header		PHY payload

Fig. 2. PPDU packet structure

the MAC after the digital demodulation performed by the proposed demodulator. The PSDU from MAC is modulated by the proposed modulator, and the resultant PPDU packet is transmitted by the RF transmitter. The details of each block are described in the following text.

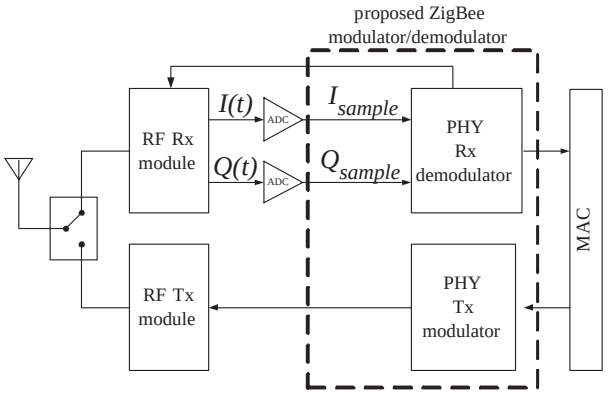

Fig. 3. Block diagram of the ZigBee transceiver for 868/915 MHz band

A. proposed ZigBee modulator

The proposed ZigBee Tx in Fig. 3 is based on [1], and its detailed block diagram is shown in Fig. 4. The PPDU packet is composed of the PSDU from MAC and the header added by the header insertion stage. The differential encoder stage encodes the PPDU packet for error correction and generates the data symbol sequence $\{S_n\}$, where $S_n \in \{-1, +1\}$. The symbol-to-chip stage performs the direct sequence spread spectrum (DSSS), where each symbol is mapped into a 15-chip pseudo-random noise (PN) sequence. The symbol "-1" and "+1" are mapped into a PN sequence, *PN_minus* and *PN_plus*, respectively, as shown in Table II. The spread data are modulated by the binary phase shift keying (BPSK) modulation. The modulated signal goes along with the pulse shaping stage to reduce the inter-symbol interference (ISI). The resultant signal is transmitted by the RF transmitter.

TABLE II

PN SEQUENCE MAPPING TABLE

	Chip values $(C_0, C_1, ..., C_{14})$
PN_minus	$+1, +1, +1, +1, -1, +1, -1, +1, +1, -1, -1, +1, -1, -1, -1,$
PN_plus	$-1, -1, -1, -1, +1, -1, +1, -1, -1, +1, +1, -1, +1, +1, +1,$

B. proposed ZigBee demodulator

Fig. 5 shows the block diagram of the ZigBee Rx. The packet detector discriminates whether the incoming signal is

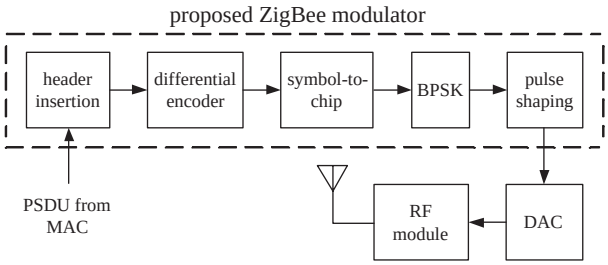

Fig. 4. Detailed block diagram of the proposed ZigBee demodulator

data or noise. It enables the following stage if the incoming signal is determined to be data. Each 15-chip PN sequence is sampled to be 60 samples by the ADC. The energy detector is in charge of positioning the chips from the samples. The frequency estimation block computes the frequency offset from samples and corrects the frequency of local oscillator by returning a control signal. The time synchronization indicates the start of each PPDU packet. With the acknowledgement of the start of the packet, the differential decoder proceeds to decode the packet. The confirm SFD stage acquires the length of the PSDU and notifies the MAC layer of receiving the PSDU from the receiver.

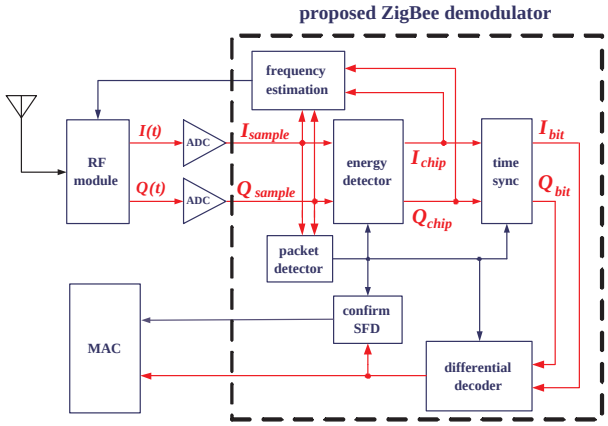

Fig. 5. Detailed block diagram of the proposed ZigBee modulator

1) Packet Detector: The absolute value of I_{sample} and Q_{sample} are accumulated for certain time interval. If the accumulated value is greater than a predefined threshold, the incoming signal is determined as data. This threshold is derived from detailed system simulations.

2) Energy Detector: The energy detector derives the positions of the chips from I_{sample} and Q_{sample}. The detailed block diagram of the energy detection is shown as Fig. 6. For the sake of simplicity, Fig. 6 only shows the processing of I_{sample}. The amplitude of each incoming samples is computed and sent to the accumulators (ACCs) sequentially. In order to reduce the complexity and power consumption, the computation of the amplitude is realized by taking the absolute value instead of the square. The Decision block finds the maximum value among the results of accumulations after a certain time interval and choose the data path with the maximum value as the chip sequence. Thus, the sample sequence is downsampled

to be a chip sequence.

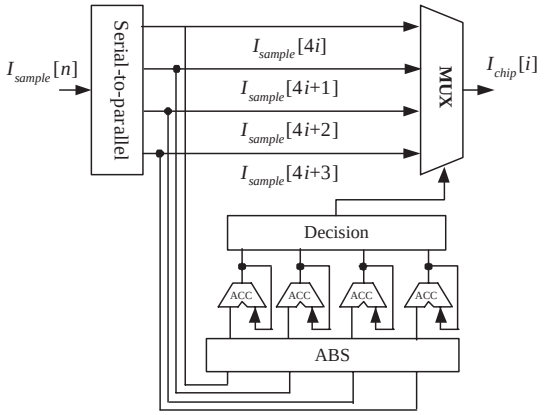

Fig. 6. Detailed block diagram of the energy detector, where $i = \lfloor n \rfloor$.

3) Frequency Estimation: The frequency estimation consists of two phases, coarse and fine estimation. The frequency estimation stage performs similar operations in these two phases such that the hardware can be reused. In the coarse phase, the frequency estimation stage calculates the average phase rotation of 128 pairs of I_{sample} and Q_{sample}. Then, it corrects the frequency of the local oscillator by returning an 8-bit control signal. In the fine phase, it uses I_{chip} and Q_{chip}, which are derived from I_{sample} and Q_{sample} by the energy detector, to calculate the average phase rotation and send an 8-bit control signal to the local oscillator.

4) Time Sync: The time sync stage performs the synchronization and the despreading function to convert the chip sequence into bit sequence. Since the preamble of the PPDU packet is designed to facilitate the synchronization, we can exploit this feature in the time sync stage. The preamble contains four octets of "0", and each "0" is spread as the PN sequence *PN_minus* as shown in the Table II. Conversely, the despreading process can be done in the Rx by recognizing each PN sequence from the received data. Such a procedure can be realized by estimating the correlation between the chip sequence and *PN_minus*, which can be expressed as follows:

$$\hat{\varepsilon}(d) = \sum_{k=0} \sum_{i=0} y_i \cdot w[i - (15 \cdot k + d)], \quad d = 0, 1, ..., 14 \quad (1)$$

and

$$w[i] = \begin{cases} PN\_minus[i], & i = 0, 1, ..., 14 \\ 0, & \text{otherwise} \end{cases} \quad (2)$$

where y_i is the received chip sequence, and w_i represents the *PN_minus* with zero padding. The k is the quotient of i divided by 15 ($\lfloor i/15 \rfloor$). The d_{opt} is the index d with the maximum $\hat{\varepsilon}(d)$, which indicates the correct start of each *PN_minus* in the preamble. Hence, the chip sequence can be despread to be a bit sequence with the acknowledgement of d_{opt} .

The time sync block utilizes the matched filter to estimate the correlation [10]. The detailed block diagram is shown as Fig. 7. The sum of the matched filters are accumulated through accumulator ACC 0 to ACC 14 sequentially. The decision circuit finds the maximum from accumulators and generates the d_{opt}.

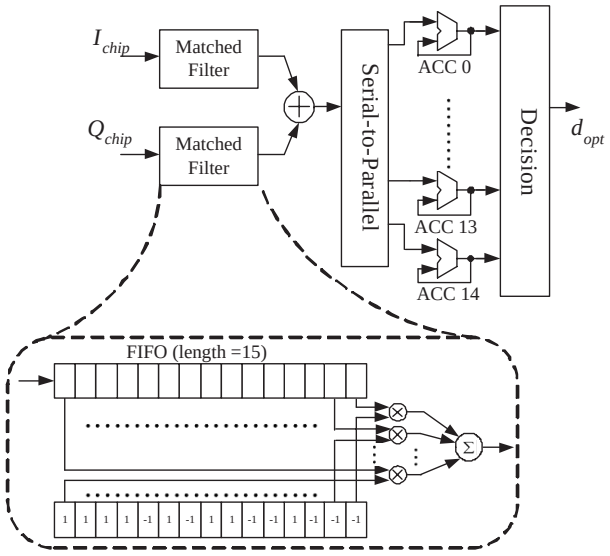

Fig. 7. Block diagram of the Time Sync block

5) Confirm SFD: The confirm SFD stage determines the frame length by acquiring the SFD field of the PPDU packet and acknowledges the MAC layer to receive the PSDU by sending an alarm signal.

III. Simulation and Measurement

The function of the proposed ZigBee transceiver for 868/915 MHz band is verified by FPGA before silicon implementation. In order to evaluate the performance and the power consumption, the proposed design is implemented by TSMC (Taiwan Semiconductor Manufacturing Company) 0.18 μm CMOS technology. All of the process corners : [0^{o}C, +100^{o}C], and (SS, TT, FF) models, are simulated. The core size is 402 μm $\times$ 402 μm, where the chip size is 1.44 mm $\times$ 1.44 mm. The die photo of proposed prototype is shown in Fig. 8.

The measurement is performed by Agilent 93000 SOC Series. The setup of the measurement follows the specification in [1], where the PSDU of each PPDU packet is set to be 20 bytes random numbers. Fig. 9 shows the comparison between simulation waveforms and measurement waveforms of the frequency estimation function, which shows the measured results exactly match the simulated results. Fig. 10 shows the measured PER of the proposed prototype, where the PER is less than 1% at SNR of 5 dB when the frequency offset of a symbol (1 symbol = 15 chips), Δf, is +80 ppm $\sim$ -80 ppm. Fig. 11(a) shows the Shmoo plot of the modulator, which shows the maximum clock rate of the modulator is 47 MHz. Meanwhile, Fig. 11(b) shows the Shmoo plot of the demodulator, which shows the maximum clock rate of the demodulator is 35 MHz. The measured power consumption of modulator/demodulator at the clock rate of 2.4 MHz is 107 μW and 144 μW, respectively. The specifications of the proposed ZigBee modulator/demodulator is summarized in Table III.

TABLE III

SPECIFICATIONS OF THE PROPOSED ZIGBEE MODULATOR/DEMODULATOR

Technology	0.18 μm CMOS process
Power supply	1.8 V
Clock rate	2.4 MHz
Power consumption of modulator at 2.4 MHz	107 μW
Power consumption of demodulator at 2.4 MHz	144 μW
core size	0.16 mm^2
Max. clock rate of modulator	47 MHz
Max. clcok rate of demodulator	35 MHz

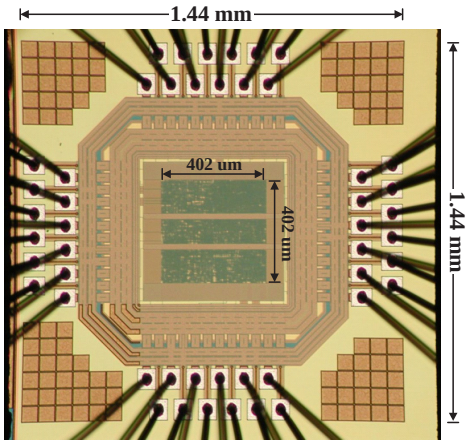

Fig. 8. Die photo of the proposed prototype

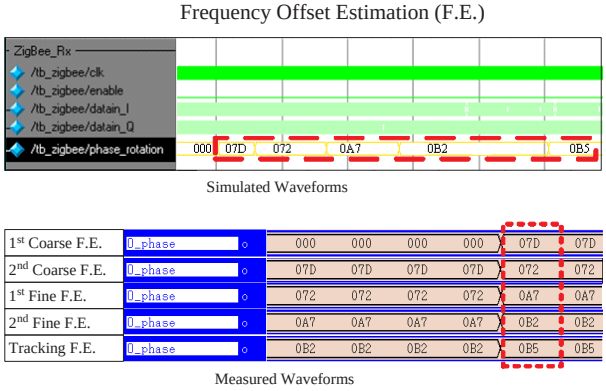

Fig. 9. Comparison between the measured waveforms and the simulated waveforms of the frequency estimation function

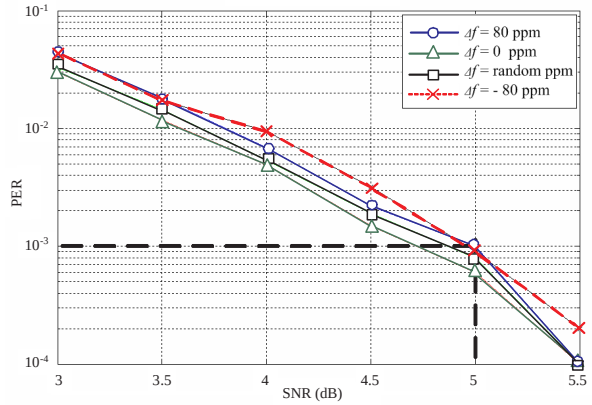

Fig. 10. PER of the proposed ZigBee Rx

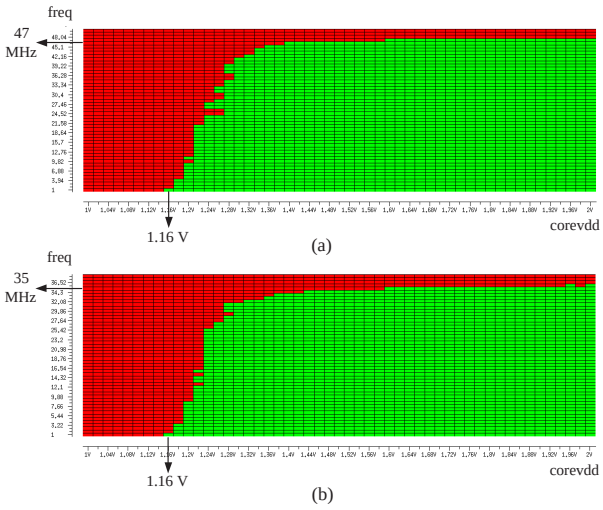

Fig. 11. Shmoo plot of the proposed design: (a) modulator and (b) demodulator

IV. CONCLUSION

In this paper, an architecture as well as hardware implementation of low power ZigBee modulator/demodulator for 868/915 MHz band is presented. The proposed ZigBee modulator/demodulator adopts the relatively simple algorithm to achieve the goal of low power and low hardware complexity without sacrificing the performance. Hence, the overall power consumption of the proposed transceiver is merely 251μW, and the area is 0.16 mm^2.

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