A Low-Power ADPLL Using Feedback DCO Quaterly Disabled in Time Domain

Chua-Chin Wang *, Chi-Chun Huang, Sheng-Lun Tseng,

Abstract

We propose a low power ADPLL (All-digital phase-locked loop) using a controller which employs a binary frequency searching method in this paper. Glitch hazards and timing violations which occurred very often in the prior ADPLL designs are avoided by the control method and the modified DCO (digital-controlled oscillator) with multiplexers. Besides, the feedback DCO is disabled half a cycle in every two cycles so as to reduce 25% of dynamic power theoretically. The proposed design is implemented by only using the standard cells of TSMC (Taiwan Semiconductor Manufacturing Company) 0.18 μm CMOS process. The feature of power saving is verified on silicon to be merely 1.53 mW at a 133 MHz output.

Key words: ADPLL, low power, glitch, timing violation, DCO.

1 Introduction

Phase-locked loops (PLLs) are widely used circuits for frequency synthesis applications. A traditional PLL consists of a digital phase frequency detector (PFD), and an analog part including a charge pump, a loop filter, and a voltage controlled oscillator (VCO). Many parameters of the analog circuits in the traditional PLL are sensitive to temperature variation, supply voltage noise as well as process drift, [1], [2]. They result in the design difficulty and the necessity of re-designing for each new technology. Moreover, capacitors and resistors, which are required in the loop filter in the traditional PLLs, [3], [4], usually cause an area penalty.

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On the contrary, ADPLL is composed of all digital components such that it possesses a high immunity to supply noise and temperature variation. Moreover, ADPLL can be designed by using hardware description language (HDL) which is applicable to any standard cell library [9]. Thus, the portability over different processes is ensured and the time for re-design is reduced. Therefore, ADPLL has been received great attention to date [6], [7], [9]. However, ADPLL has a crucial disadvantage, i.e., large power consumption resulting from the digital-controlled oscillator (DCO), as shown in Table 1. For instance, the ADPLL for high-speed clock generation proposed by Chung [5] consumes 100 mW at 500 MHz, which does not follow the trend of low power design. Moreover, it may introduce glitches into the oscillator due to switching delays.

	Traditional PLL	ADPLL
Design time	Long	Short
Reusability	Bad	Good
Noise immunity	Bad	Good
Area	Large	Small
Power consumption	Small	Large

Table 1
Performance comparison between the traditional PLL and ADPLL.

Thus, we propose a novel binary frequency searching control method for ADPLL to reduce the power consumption caused by DCO and avoid glitch hazards. Meanwhile, the feedback DCO can be stopped half a cycle in every two consecutive cycles to further reduce power dissipation. The power consumption of the proposed ADPLL is found to be merely 1.53 mW at 133 MHz output.

2 ADPLL with low-power control

Referring to Fig. 1, the proposed ADPLL is composed of a PFD, a frequency divider (FDIV), two DCOs (FB_DCO and OUT_DCO), and the controller for saving power (CSP). PFD detects the phase difference between the reference clock CLK_REF and the feedback clock CLK_FB. When CLK_FB lags CLK_REF, PFD generates a negative impulse on UP while DOWN remains at high to sigal CSP to speed up the FB_DCO. On the contrary, a negative impulse on DOWN is generated to slow down FB_DCO if CLK_FB leads

CLK_REF. CSP generates two signals, COARSE and FINE, for FB_DCO to select an oscillation frequency of CLK_FB_M. The frequency of CLK_FB_M is divided by the FDIV with a division ratio MOD to generate the divided signal CLK_FB which is sent back to PFD.

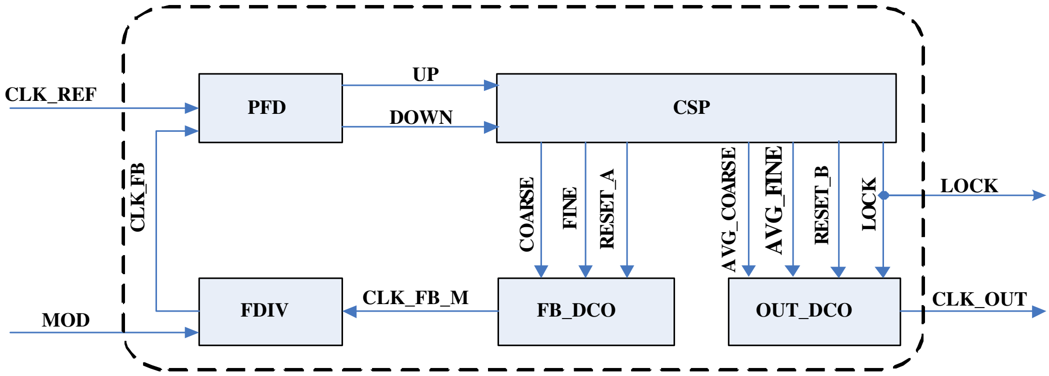

Fig. 1. Block diagram of the proposed ADPLL.

After the coarse tune and the fine tune steps, a stable feedback loop is settled. The frequency of CLK_FB_M is adjusted to be MOD times of that of CLK_REF. Simultaneously, a signal LOCK is generated by CSP to indicate the frequency is locked successfully. In order to further reduce the jitter caused by (1) PFD's deadzone, (2) the FB_DCO's finite resolution, and (3) the input jitter, CSP computes the averaged values of COARSE and FINE, i.e., AVG_COARSE and AVG_FINE, respectively, for OUT_DCO to generate the stable output signal CLK_OUT.

2.1 The PFD and the FDIV

Fig. 2 shows the schematic of PFD [5]. The PFD generates a low impulse on UP or DOWN according to the lag or lead of CLK_FB relative to CLK_REF, respectively. Notably, the impluse itself, not the width of the impulse, is used to the invoke the speed-up or slow-down event in the CSP.

Two digital pulse amplifiers (DPAs), as shown in Fig. 3, are used to increase the pulse width of INTU and INTD such that the following D-filp-flops (DFFs), DFF3 and DFF4, can detect them [5]. Thus, the dead zone of the PFD can be effectively minimized. Moreover, in order to increase the sensitivity to the input phase difference, asynchronous resets are adopted in DFF1 to DFF4. However, the asynchronous reset may cause the timing violation happened in these DFFs if CLK_FB and CDN, where CDN is the feedback clear signal to DFF1 and DFF2, possess contradictive values, namely "conflict", shown in Fig. 4. This "conflict" problem can be avoided by the proposed control method, which make CLK_FB rise earlier away from the rising edge

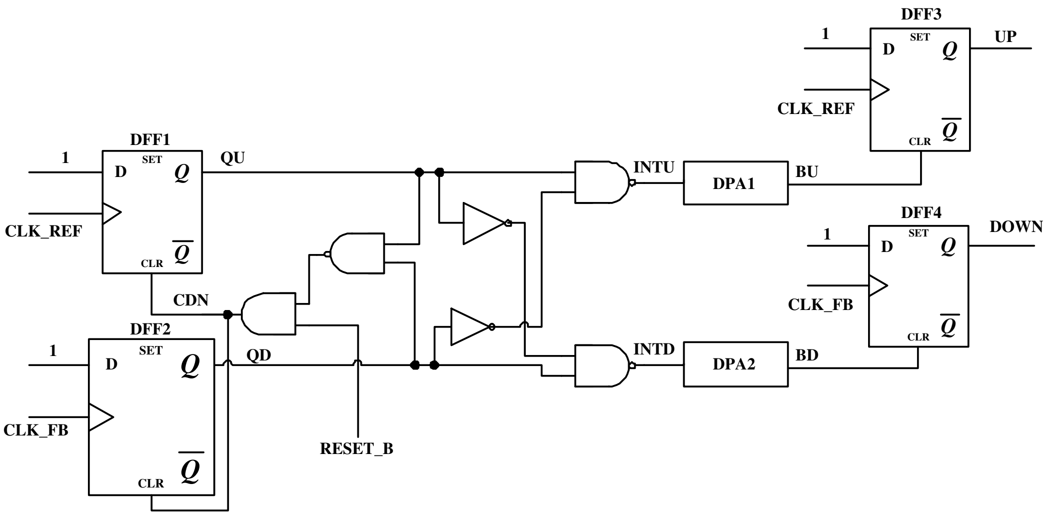

Fig. 2. Schematic of the PFD.

of CDN by resetting FB_DCO in every search step.

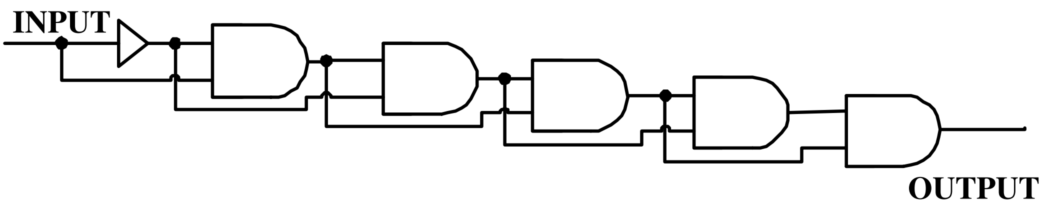

Fig. 3. Schematic of the digital pulse amplifier.

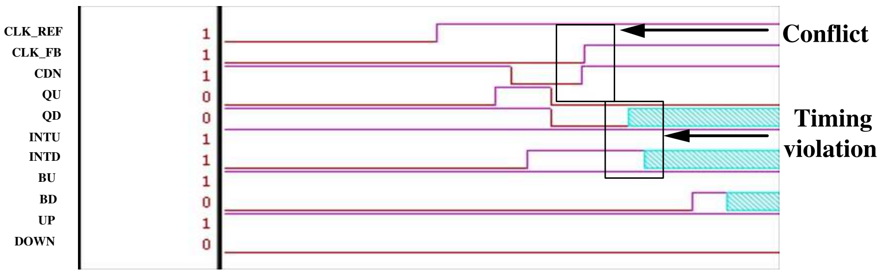

Fig. 4. Timing violation on QU and QD.

FDIV is realized based on a 4-bit counter to provide a variable division ratio, MOD, by users. In addition, FDIV is also designed with synthesizable HDL (Hardware Describe Language) code which decreases the design cost of migration among different cell libraries.

2.2 The DCOs with MUX-based Switching

The DCOs, FB_DCO and OUT_DCO, are composed of COARSE_TUNE and FINE_TUNE delay cells, as shown in Fig. 5. The reset signals, RESET_A or RESET_B, receive a low impulse to initiate the DCOs. The control codes, COARSE and FINE, switch the COARSE_TUNE and FINE_TUNE delay cells, respectively, to select the desired oscillating frequency, as shown in Fig. 6. In Chung's design, tri-state buffers were used to switch the delay cells [5] which might cause timing violations in post-layout simulations. The reason is that the "high-Z" state created by tri-state buffers will be fed back to the the rest of the ADPLL if the input phases of two tri-state buffers were different. As a result, it will crash the whole post-layout simulation. Instead, we propose to utilize multiplexers to switch the delay cells to resolve this problem. A rising edge of the input signal of the multiplexer is pre-set to wait for COARSE and FINE signals to switch the delay line such that the timing violation can be avoided.

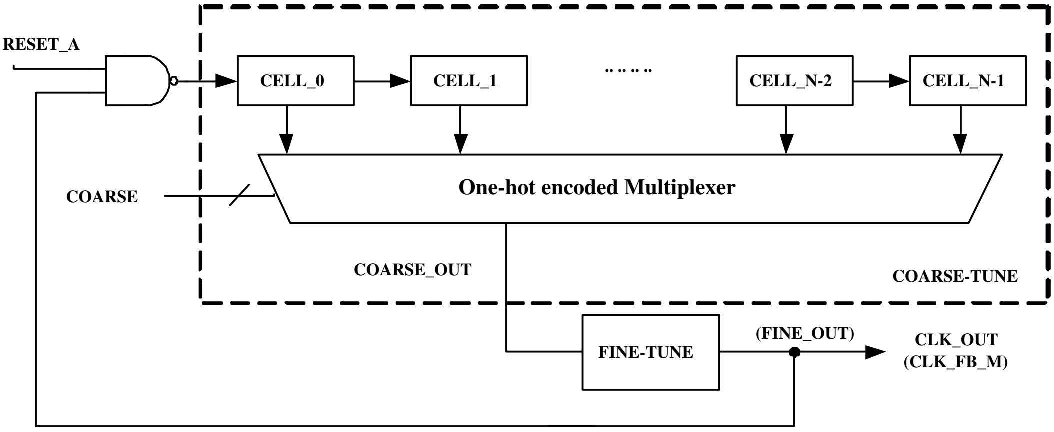

Fig. 5. Schematic of the DCOs.

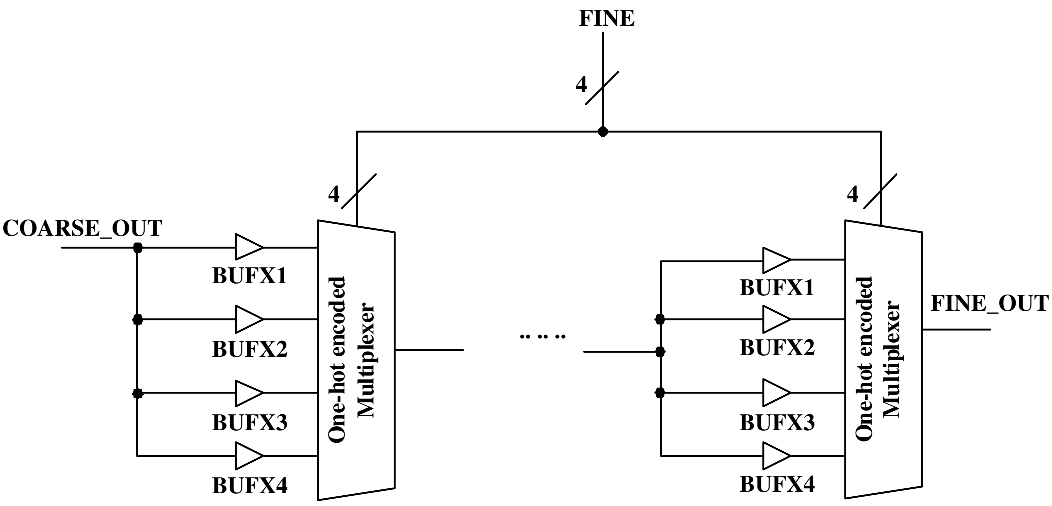

Fig. 6. Schematic of FINE_TUNE cells.

Nevertheless, a glitch will appear at the output of DCOs if the switched inputs of the multiplexers does not rise simultaneously. What even worse is that the glitch would be accumulated over the feedback loop resulting in the chaos on the outputs of FB_DCO, as shown in Fig. 7. The glitches can be removed by the proposed control method, that disable FB_DCO every time when multiplexer is switched after a searching step.

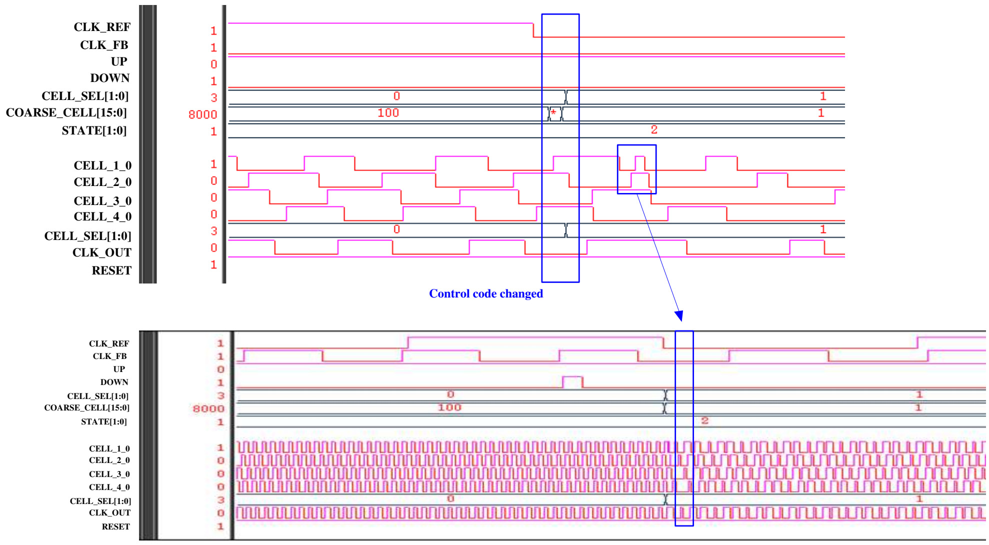

Fig. 7. The glitch on CLK_FB_M due to the accumulated phase error.

2.3 CSP with Binary Frequency Searching

The state diagram of the proposed low-power controller is divided into four states, Start, COARSE-TUNE, FINE-TUNE, and LOCK, as shown in Fig. 8.

2.3.1 Start state

The controller is initialized at the Start state and then triggered by the UP and DOWN signals from PFD to move to other states.

2.3.2 COARSE-TUNE state

In this state, the 5-bit COARSE code are computed by a binary search, as shown in Fig. 9, to adjust the frequency of FB_DCO. FB_DCO starts from the middle of its frequency range. The frequency is increased if a low impulse on UP is received. Otherwise, the frequency is slowed down if a low impulse on DOWN is received. When each bit of COARSE is determined, the counter COARSE_STEP, which is used to count the binary search for COARSE, decreases by one from the number of the bit size of COARSE. Smaller the COARSE_STEP is, the frequency of CLK_FB is closer to CLK_REF. When the COARSE_STEP reaches 1, it means the closest COARSE code is found.

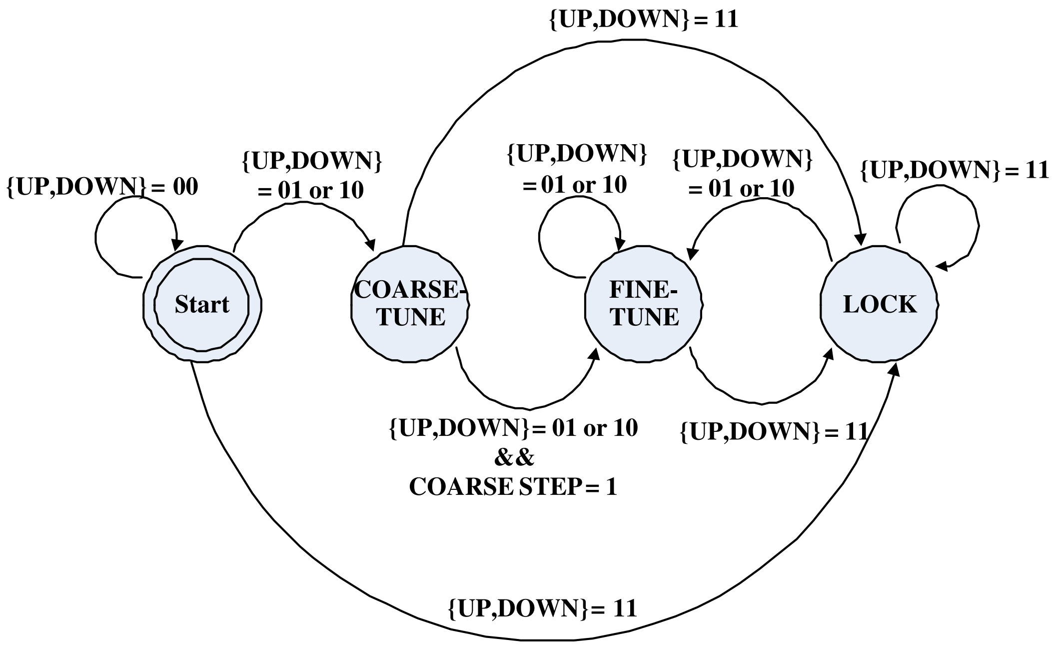

Fig. 8. The state diagram of the proposed CSP.

This COARSE code searching procedure continues until either of the following two events happen.

2.3.2.1) When the COARSE_STEP equals to 1 and [UP, DOWN]=10 or 01, the controller moves to the FINE_TUNE state to compute the 4-bit FINE codes.

2.3.2.2) When UP and DOWN are both high, the target frequency is found. The controller goes to the LOCK state.

2.3.3 FINE-TUNE state

The search step of the FINE_TUNE state is the same as the CORASE_TUNE state except that no counter is required to count the search step.

2.3.4 LOCK state

The CSP computes the averaged value over the prior 64 cycles of COARSE and FINE. The two average values, AVG_COARSE and AVG_FINE, are sent to OUT_DCO to generate the output clock CLK_OUT. Besides, a signal LOCK is activated to enable OUT_DCO and to indicate that the target frequency is found.

The proposed low-power control method to switch the frequency of FB_DCO

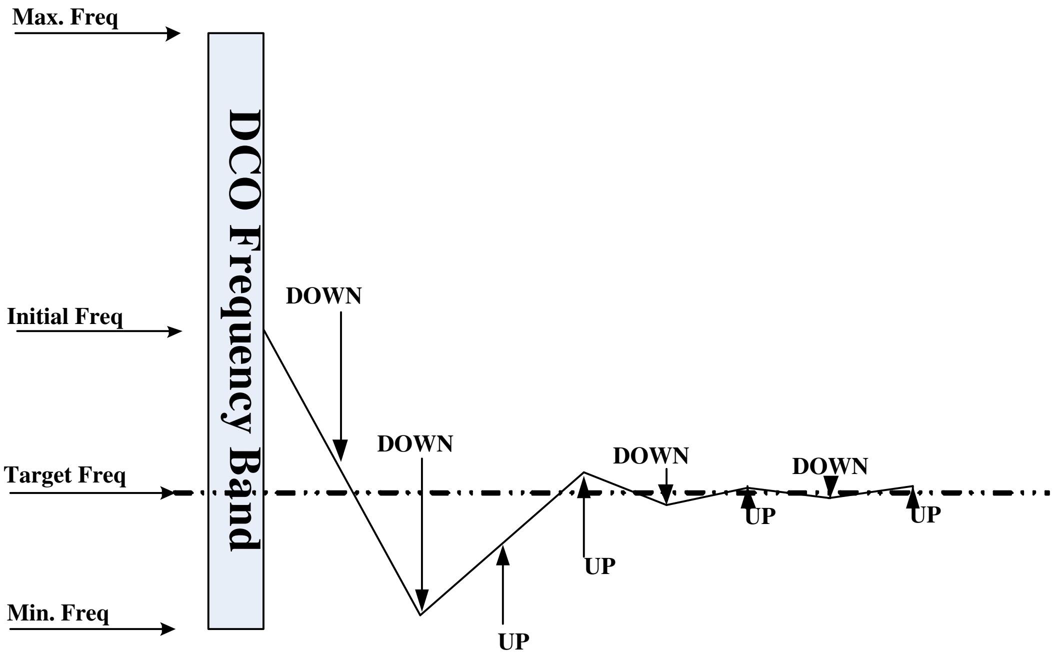

Fig. 9. The binary search for the target frequency.

for the binary search is addressed as follows. At the rising edge of the first cycle, i.e., "A" in Fig. 10, CSP enables FB_DCO by setting RESET_A to attain the simultaneous rising edges of CLK_FB and CLK_REF. At the rising edge of the second cycle ("B" in Fig. 10), CSP receives the detected phase error of CLK_FB and CLK_REF from PFD. At the falling edge of the second cycle ("C" in Fig. 10), CSP sends the computed COARSE or FINE codes according to the received UP or DOWN to select the frequency of CLK_FB_M, and disables FB_DCO at the same time. Repeatedly, FB_DCO is disabled every time when the delay line is switched. Thus, the conflict problem and the glitch on CLK_FB_M are avoided. Notably, two cycles of CLK_FB_M are needed to complete a search step for the frequency of CLK_FB.

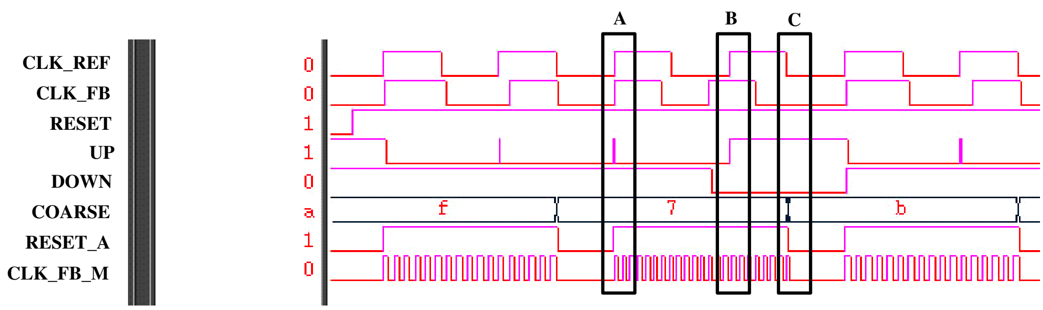

Fig. 10. The simulation result of the proposed CSP.

What even better is that the proposed control method disables FB_DCO half cycle in every two clock cycles. It saves 25% dynamic power besides getting rid of the conflict problem and annoying glitches of CLK_FB_M. Notably, these glitches might be accumulated over the feedback loop and finally crash the function of the whole chip.

	ours	[5]	[6]	[8]	[9]
Technology	0.18 μm CMOS	0.35μm CMOS	0.35μm CMOS	0.5μm CMOS	0.6μm CMOS
Design approach	cell-based	cell-based	cell-based	Full-custom	cell-based
Area	0.06 mm^2	0.71 mm^2	0.07 mm^2	1.1 mm^2	2.75 mm^2
Power consumption	1.53 mW @133 MHz	100 mW @500 MHz	8.1 mW @152 MHz	39.6 mW @100 MHz	315 mW @800 MHz
Power delay product	11.48 ns·mW	200 ns·mW	53.46 ns·mW	396 ns·mW	393.75 ns·mW
Index of Power	1.00	1.29	1.25	9.00	9.32
Max. freq.	158 MHz	510 MHz	336 MHz	550 MHz	800 MHz
Min. freq.	70 MHz	45 MHz	152 MHz	50 MHz	360 MHz
Supply voltage	1.8 V	3.3 V	3.0 V	3.3 V	3.3 V
Output jitter (pk-pk)	300 ps	70 ps	1.2 ns	125 ps	60 ps
Figure of Merit	162	65	8.5	18.4	23.3

Table 2
Specifications comparison of the proposed ADPLL.

3 Implementation and Measurement

The proposed ADPLL is carried out by using TSMC 0.18 μm 1P6M CMOS process standard cells with 1.8 V power supply. In order to achieve the timing accuracy, we use Verilog hardware description language to directly select the cells from TSMC standard cells.

The post-layout simulation in Fig. 11 shows the phase detection process of PFD, where no timing violation is occurred in contrast with the scenario in Fig. 4. Fig. 12 shows the simulation results of the proposed ADPLL, where the reference clock is 10 MHz, the division ratio MOD is 12, and the ourput frequency is 125 MHz. Moreover, there is no glitch or timing violation regarding CLK_FB_M and any other signal.

Fig. 13 shows the die photo of the proposed ADPLL on silicon. The result of measurement, given the same condition as simulations, is shown in Fig. 14. Not only is the waveform correct as the simulation results, the output frequence

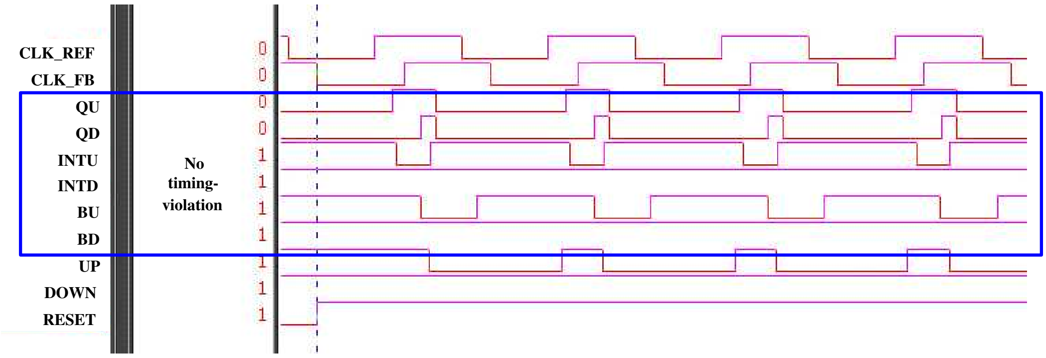

Fig. 11. The post-layout simulation result of PFD.

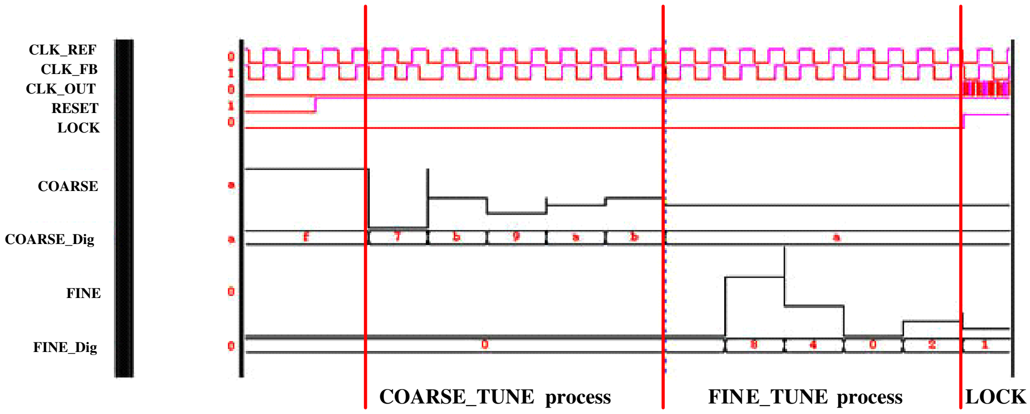

Fig. 12. The post-layout simulation result of the proposed ADPLL.

also matches with the reference frequnece by FFT analysis. The spectrum of the output frequency is shown in Fig. 15.

Table 2 summarizes the comparison of the proposed ADPLL with several prior works. The frequency range of the proposed design is unavoidably reduced due to the extra delay caused by the multiplexers. By contrast, the power consumption, the power delay product, and the normalization index of power consumption vs. process, supply voltage and frequency of our design is the best of all listed design, as well as the FOM (Figure of Merit defined in Eqn. (1)). In other words, the proposed design gains the edge of power consumption with a reasonable sacrifice of the output ferquency.

$$\text{Figure of Merit} = \frac{\frac{(Max.\ freq.)\ -\ (Min.\ freq.)}{Max.\ freq.}}{jitter \cdot (power\ delay\ product)} \quad (1)$$

The denominator in the right-hand side of Eqn. (1) denotes the product of the jitter and the power-delay product, which is supposed to be the smaller the better for the ADPLL. By contrast, the numerator in the right-hand side of Eqn. (1) is the dynamic bandwidth ratio (dynamic bandwidth range vs.

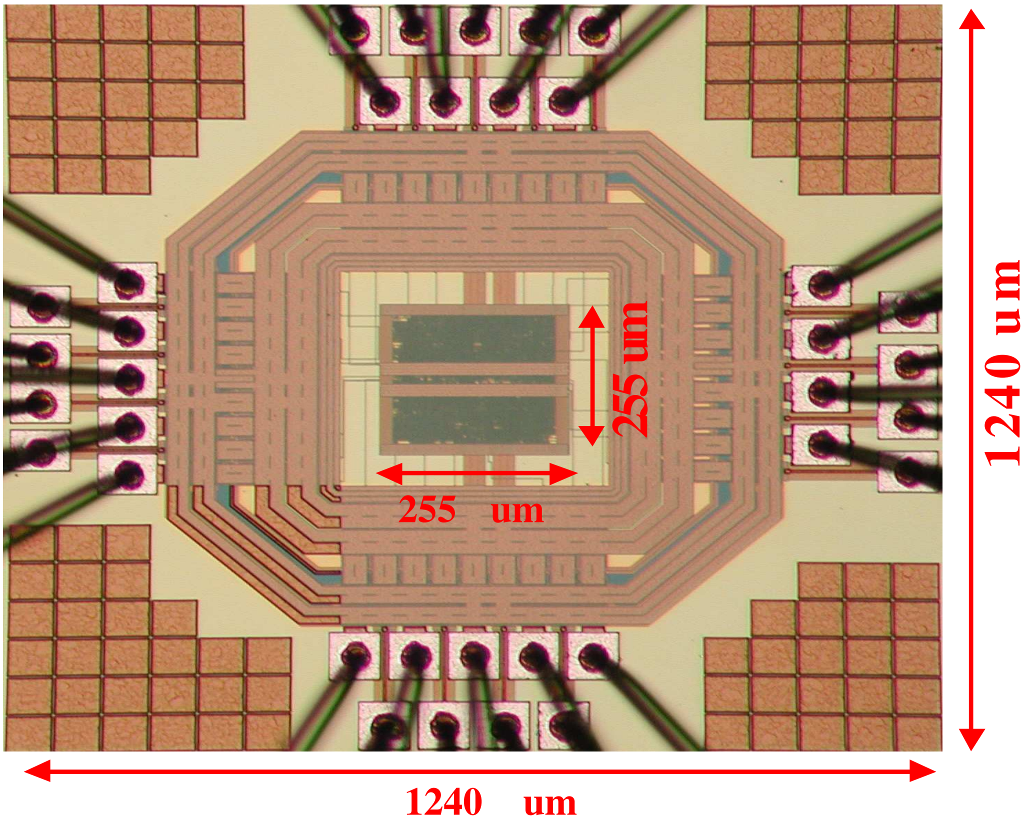

Fig. 13. Die photo of the proposed ADPLL.

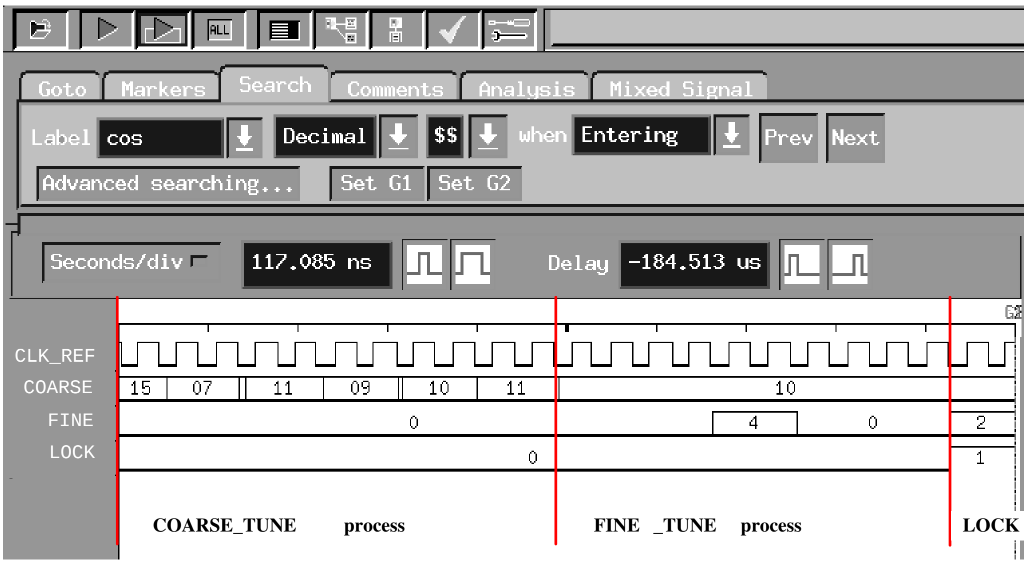

Fig. 14. The measurement result of the proposed ADPLL.

maximum output frequency), which should be the larger the better for the ADPLL.

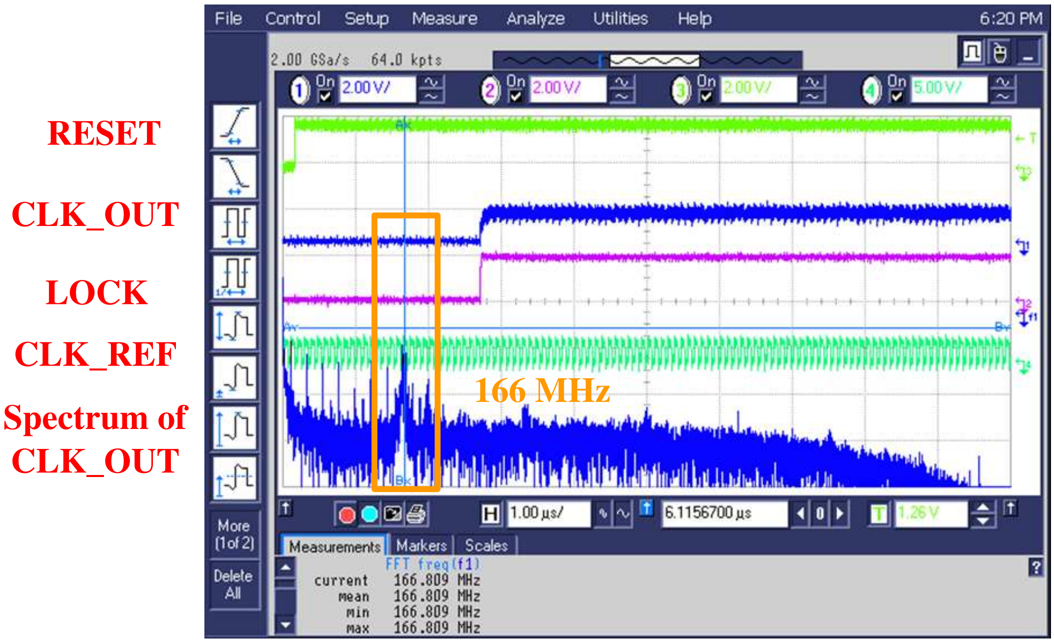

Fig. 15. The spectrum of the output frequency with 166 MHz CLK_REF.

4 Conclusion

We have presented a low power ADPLL by using a binary frequency searching method. Moreover, the glitch hazard and the timing violation in the prior works are avoided by the proposed control method and the modified DCOs with multiplexers. Notably, the power dissipation caused by the feedback DCO is reduced, since it is disabled quarterly in the time domain. The feacture of saving power is verified by the measurement on silicon, which shows that the power consumption of the proposed ADPLL is merely 1.53 mW.

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References

[1] T.-D. Chiueh, J.-B. Yang, and J.-S. Wu, "Design and Implementation of a Low-Voltage Fast-Switching Mixed-Signal-Controlled Frequency Synthesizer," *IEEE Trans. Circuits Systems II,* vol. 48, no. 10, pp. 961-971, Oct. 2001.

[2] R. Nonis, N.D. Dalt, P. Palestri, and L. Selmi, "Modeling, design and characterization of a new low jitter analog dual tuning lc-vco pll architecture," *Inter. Symp. on Circuits and Systems(ISCAS '98),* vol. 4, pp. 23-26, May. 2005.

[3] R. Nonis, N.D. Dalt, P. Palestri, and L. Selmi, "Modeling, design and characterization of a new low jitter analog dual tuning lc-vco pll architecture," *IEEE J. Solid-State Circuits,* vol. 40, no. 6, pp. 1303-1309, Jun. 2005.

[4] A.-M. Fahim, and M.-I. Elmasry, "A Fast Lock Digital Phase-Locked-Loop Architecture for Wireless Applications," *IEEE Trans. Circuits Systems II,* vol. 50, no. 2, pp. 63-72, Feb. 2003.

[5] C.-C. Chung, and C.-Y Lee, "An All-Digital Phase-Locked Loop for High-Speed Clock Generation," *IEEE J. Solid-State Circuits,* vol. 38, no. 2, pp. 347-351, Feb. 2003.

[6] T. Olsson, and P. Nilsson, "A digitally controlled PLL for SoC applications," *IEEE Journal Solid-State Circuits,* vol. 39, no. 5, pp. 751-760, May 2004.

[7] J.-S. Chiang, and K.-Y Chen, "The design of an all-digital phase-locked loop with small DCO hardware and fast phase lock," *IEEE Trans. Circuits Systems II,* vol. 46, no. 7, pp. 945-950, July 1999.

[8] J. Dunning, G. Garcia, J. Lundberg, and E. Nuckolls, "An all-digital phase-locked loop with 50-cycle lock time suitable for high-performance microprocessors," *IEEE J. Solid-State Circuits,* vol. 30, no. 4, pp. 412-422, Apr. 2004.

[9] T.-Y. Hsu, C.-C. Wang, and C.-Y. Lee, "Design and analysis of a portable high-speed clock generator," *IEEE Trans. Circuits Systems II,* vol. 48, no. 4, pp. 367-375, Apr. 2001.

Figure Captions

Fig. 1 Block diagram of the proposed ADPLL.

Fig. 2 Schematic of the PFD.

Fig. 3 Schematic of the digital pulse amplifier.

Fig. 4 Timing violation on QU and QD.

Fig. 5 Schematic of the DCOs.

Fig. 6 Schematic of FINE_TUNE cells.

Fig. 7 The glitch on CLK_FB_M due to the accumulated phase error.

Fig. 8 The state diagram of the proposed CSP.

Fig. 9 The binary search for the target frequency.

Fig. 10 The simulation result of the proposed CSP.

Fig. 11 The post-layout simulation result of PFD.

Fig. 12 The post-layout simulation result of the proposed ADPLL.

Fig. 13 Die photo of the proposed ADPLL.

Fig. 14 The measurement result of the proposed ADPLL.

Fig. 15 The spectrum of the output frequency with 166 MHz CLK_REF.