efficiency and little side effects of this kind of treatment method. With the aforementioned benefits, PMCT will be widely used in treating different tumors. In this letter, the principle and geometry of one improved MPC system are investigated in this article; the main parts of the system are briefly introduced. The improved MPC takes the features of convenience of operation and maintenance. A large number of experiments on porcine liver are carried out, and the temperature distribution within the liver are measured and illustrated, for cases of different injected microwave power and ablation time. Based on a large amount of measured data from the in-vitro experiments, the graphics of the coagulation area in porcine livers are reconstructed, demonstrating obvious change from conglobulation to ellipsoid. The minimum diameter of coagulation area is about 2 cm, and it can reach 6 cm with the increase of microwave output power of the instrument (i.e., MPC), while the transverse diameter can reach ~3.5 cm. These experimental researches can probably provide some useful reference to the clinic treatment of the liver cancer using MPC system.

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A CMOS OPTO-ELECTRONIC SINGLE CHIP USING THE HYBRID SCHEME FOR OPTICAL RECEIVERS

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ABSTRACT: *An opto-electronic integrated circuit based on the hybrid scheme for an optical receiver front-end is presented in this article. The proposed integrated circuit adopts the CMOS technology as the vehicle to integrate the InP-based waveguide photodetector into the transimpedance amplifier (TIA) circuit. A regulated cascade structure is used to reduce the input impedance of the TIA. Hence, the proposed integrated circuit can achieve a very high bandwidth provided that the parasitic capacitance of the photodetector is up to 1 pF. The 3-dB bandwidth and the transimpedance gain of the proposed circuit are 1 GHz and 64.5 dBΩ, respectively.* © 2008 Wiley Periodicals, Inc. Microwave Opt Technol Lett 50: 2430–2434, 2008; Published online in Wiley InterScience (www.interscience.wiley.com). DOI 10.1002/mop.23693

Key words: *photodetector; transimpedance amplifier; regulated cascade; OEIC*

1. INTRODUCTION

The CMOS technology has been a promising solution for the Si-photonics integrations because of low cost, high yield, and capability to realize the mass production. However, the poor light-generating property of the silicon material makes the optical component hard to be implemented by the CMOS technology. On the contrary, the materials which possess the efficient light generation, such as III-V quantum, will suffer from the poor mobility of carriers. Thus, the integration of the conventional opto-electronic integrated circuits (OEICs) is usually realized on a board level, and consequently the frequency response will be degraded by the serious parasitics.

To eliminate the burden on the frequency response imposed by the board-level integration, a more effective scheme is to carry out the integration on a chip scale. The schemes for the chip-scale integration in recent researches are mainly focused on two schemes: the monolithic scheme [1, 2] and the hybrid scheme. The monolithic scheme usually adopts the III-V material as the substrate to fabricate the optical components. Then, selective area etching is employed to define an area for regrow-

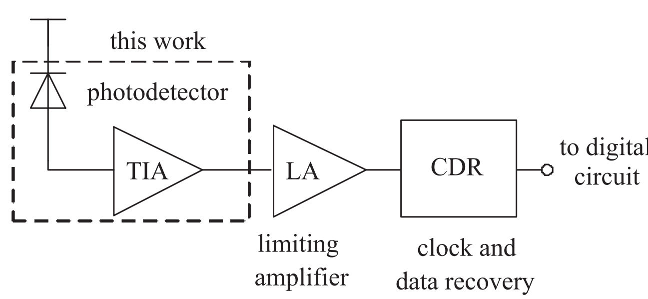

Figure 1 The architecture of a conventional optical receiver front-end

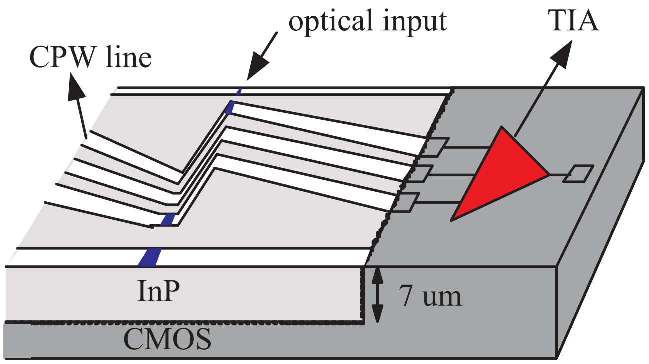

Figure 2 The structure of the proposed optic-electronic integrated circuits. [Color figure can be viewed in the online issue, which is available at www.interscience.wiley.com]

ing the electronic components. Although the monolithic scheme can realize the integration on a single substrate, the III-V technology can not compete with the CMOS technology in terms of the yield, the cost, and the volume of circuits. On the contrary, the hybrid scheme uses different technologies to fabricate the optical components and the electronic components, respectively. Then, all of the components are integrated by wafer bounding. As the choice of the technology for each component is not limited to the same material, the performance of the hybrid scheme is considered to be better than the monolithic scheme.

The hybrid scheme platform has been recently proven as an excellent solution to the integration of optical elements and passive electronic elements [3–5]. However, the realization of the OEICs based on the hybrid scheme has never been physically demonstrated in prior works. This article presents an OEIC that integrates the InP photodetector and the CMOS transimpedance amplifier (TIA) circuit into a single chip.

2. DESIGN OF THE PROPOSED OEIC BASED ON THE HYBRID SCHEME

Figure 1 shows the architecture of a conventional optical receiver, where the optical input is converted into a tiny photocurrent by the photodetector, which is then amplified as a voltage signal by the TIA. As the input stage of the optical receiver, the TIA dominates the overall bandwidth and noise performance. Besides, the input impedance of the TIA must be small enough to avoid the bandwidth being dominated by the input pole resulted from the large junction capacitance of the photodiode.

Figure 2 depicts the structure of the proposed opto-electronic circuit on a single chip for optical communication applications, where an InP-based waveguide photodetector and a CMOS TIA circuit are integrated on a single substrate. The TIA circuit is implemented by a standard 0.35-μm CMOS technology. A portion of the area with the depth of 7 μm is removed by selective etching to expose the silicon substrate for wafer bounding. The waveguide photodetector with a 7 μm thickness is bounded onto the CMOS silicon substrate. The photocurrent generated by the waveguide photodetector is coupled to the TIA circuit via the coplanar waveguide (CPW) line, where the CPW lines are arranged as a G-S-G (ground-signal-ground) type to shield the photocurrent signal.

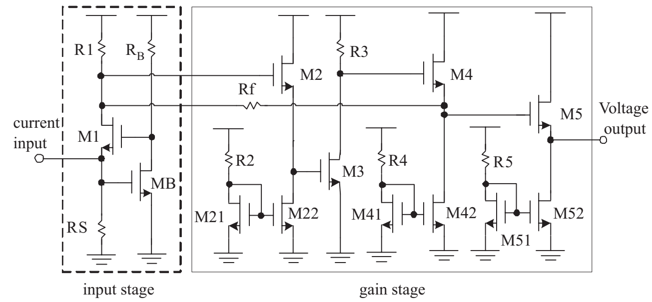

Figure 3 The schematic of the TIA circuit

Figure 3 shows the schematic of the TIA circuit adopted in this work, which is composed of an input stage and a gain stage. The input stage is in charge of converting the photocurrent signal into a voltage signal. The gain stage provides a sufficient gain to amplify the voltage signal. Because the stability and the bandwidth are our primary concerns in the TIA design, a feedback network constructed by Rf is introduced to extend the bandwidth and lower the noise. The input stage is a regulated cascade (RGC) circuit [6], which has the characteristics of small input impedance, large output impedance, and large bandwidth. The transistor M1 converts the input current into a voltage signal, where a local feedback loop composed of M1 and MB reduces the input impedance. The input impedance of the RGC circuit can be expressed as

$$Z_{\mathrm{in}}(0) \cong 1/g_{ml}(1 + g_{m\mathrm{B}}R_{\mathrm{B}}), \quad (1)$$

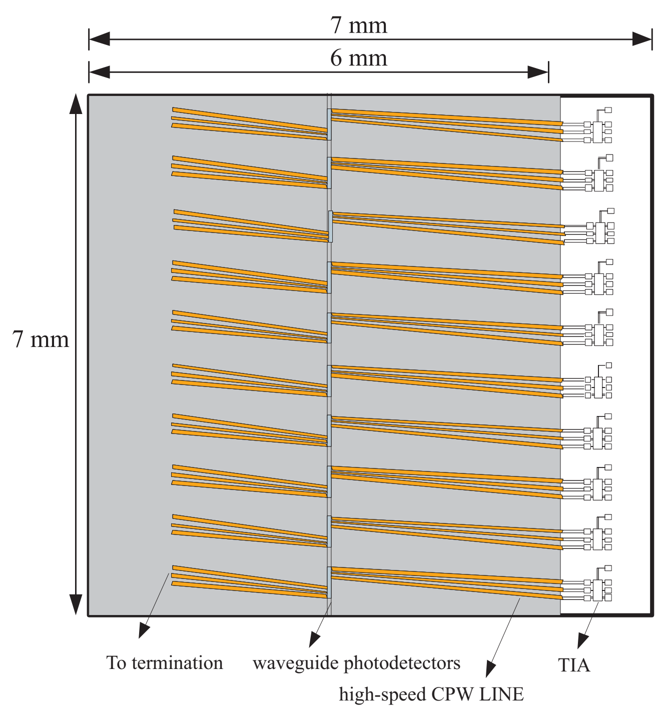

Figure 4 The layout of the proposed OEIC. [Color figure can be viewed in the online issue, which is available at www.interscience.wiley.com]

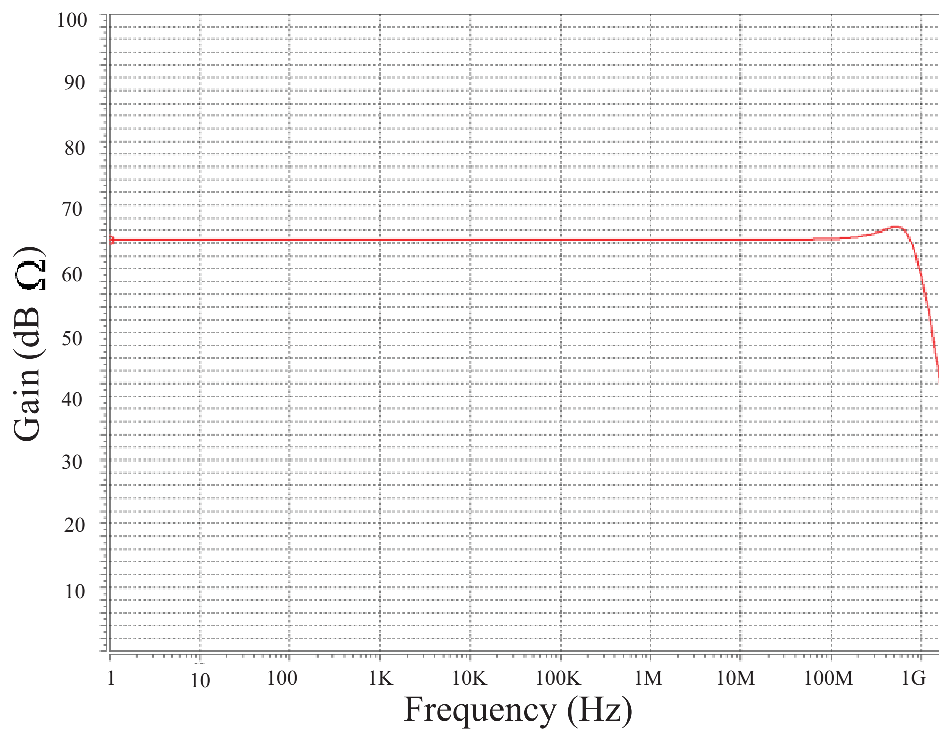

Figure 5 The simulation result of the proposed TIA. [Color figure can be viewed in the online issue, which is available at www.interscience.wiley.com]

where the g_{m1} is the transconductance of M1. According to Eq. (1), we can find the input impedance to be very small to virtually isolate the large parasitic capacitance of the photodetector.

The gain stage is composed of three common drain (CD) amplifiers and a common source (CS) amplifier. The last two CD amplifiers consist of a voltage buffer to drive the load. The first CD amplifier shifts the output signal of the input stage to a proper voltage level for the following *n*-type CS amplifier which has a higher mobility. Besides, the small parasitic capacitance C_{gd} can also prevent the pole at the input node of the first CD amplifier from dominating the BW due to the large output resistance of the RGC circuit.

3. IMPLEMENTATION

The proposed work adopts the hybrid scheme to implement a opto-electronic integrated circuit, where the CMOS-based platform and the TIA circuit are carried out by a standard 0.35-μm CMOS technology. The photodetector is realized by using the InP-based waveguide photodetector. Figure 4 shows the layout of the proposed OEIC, where the die area of the silicon part is 7 × 7 mm^2, including a TIA array (7 × 1 mm^2) and a substrate for wafer bounding (7 × 6 mm^2). An InP-based waveguide photodetector with the area of 7 × 6 μm^2 is aligned to the TIA circuits and then is bounded to the substrate.

Figure 5 shows the transimpedance gain and the 3-dB bandwidth of the TIA, where the transimpedance gain and 3-dB bandwidth are found to be 64.5 dBΩ and 1.02 GHz, respectively. Figure 6 shows the input impedance and the output impedance of the TIA, where the input impedance and the output impedance are 49.5 and 77.1 Ω, respectively. Figure 7 shows the eye diagram at 1 Gbps for a given 2^{15}-1 pseudo-random binary sequence (PRBS) input, where the height and width of the eye are 160 mV and 920 ps, respectively. Table 1 shows the comparison of the TIA with several prior works. Though capacitance of the photodetector is up to 1 pF, the proposed design can still achieve a desirable 3-dB bandwidth. However, the proposed design possesses the largest transimpedance gain compared with the prior works.

4. CONCLUSION

An opto-electronic integrated circuit based on the hybrid scheme for optical receivers is proposed in this article. The proposed circuit integrates the InP-based waveguide photodetector into the CMOS-based platform, which can provide a low cost, high-speed optical-to-electrical (EO) conversion. To resolve the difficulties emerged in the EO conversion, the RGC circuit is adopted to reduce the input impedance. Hence, the proposed integrated circuit can realize both the low input impedance and high bandwidth without sacrificing any transimpedance gain.

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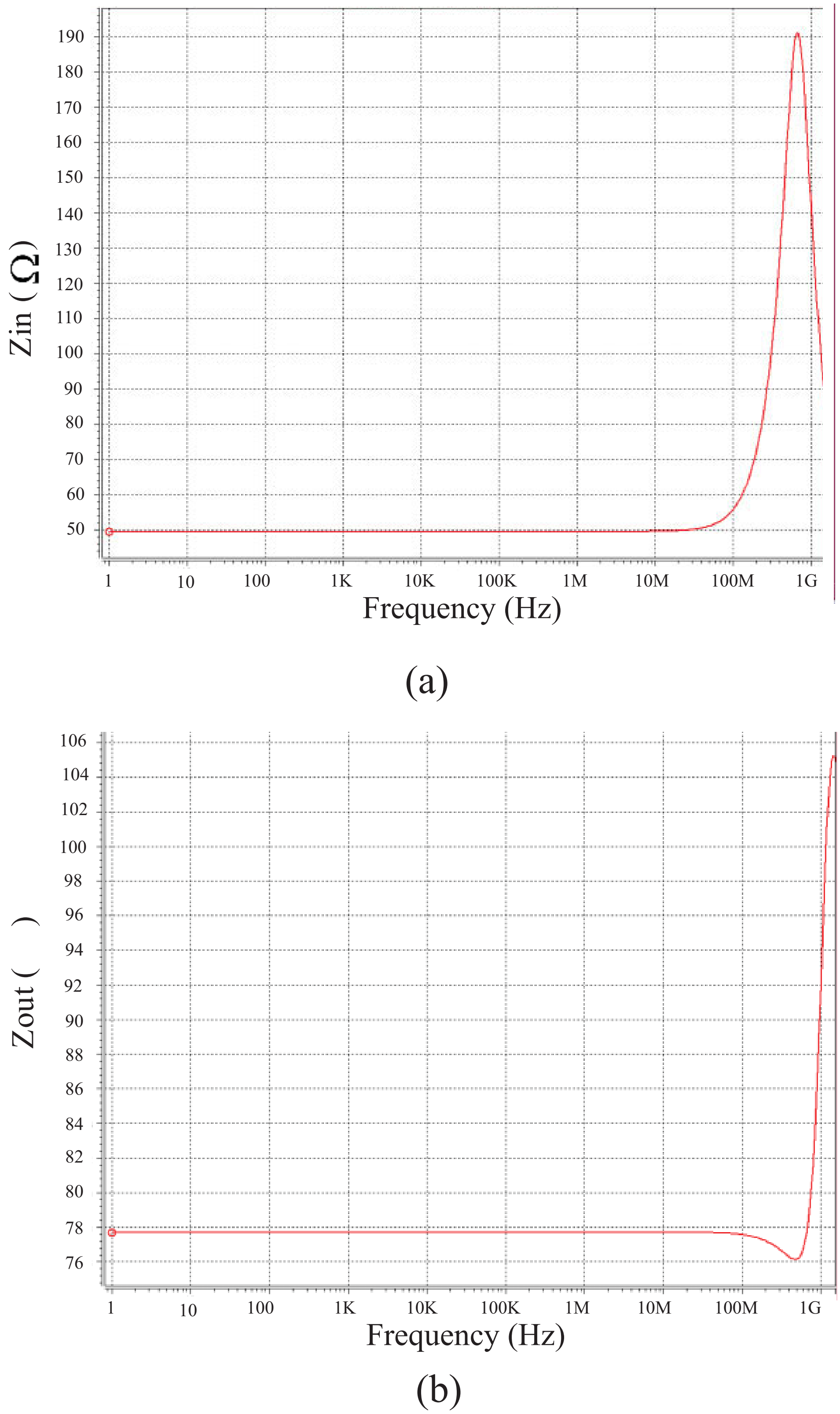

Figure 6 (a) The simulated input impedance of the TIA. (b) The simulated output impedance of the TIA. [Color figure can be viewed in the online issue, which is available at www.interscience.wiley.com]

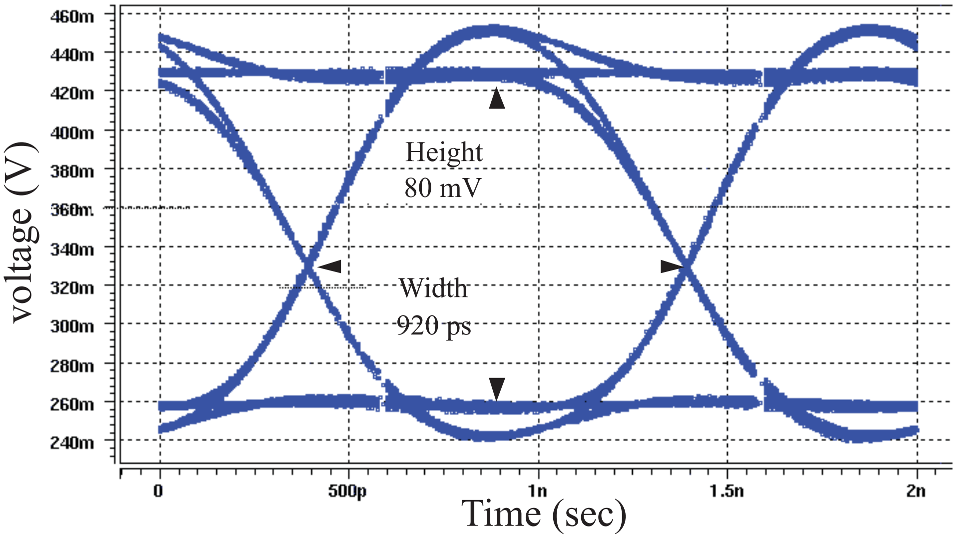

Figure 7 The eye diagram of the TIA given the $2^{15} - 1$ PRBS input. [Color figure can be viewed in the online issue, which is available at www.interscience.wiley.com]

TABLE 1 Comparison of the Proposed Circuit with Prior Works

	[7]	[8]	[9]	[6]	This work
Technology	0.35 μm	0.5 μm	0.8 μm	0.6 μm	0.35 μm
3-dB Bandwidth	1.35 GHz	1.2 GHz	660 MHz	860 MHz	1.02 GHz
Photodiode capacitance	N/A	0.6 pF	0.32 pF	1 pF	1 pF
Transimpedance gain	501 Ω	800 Ω	1120 Ω	800 Ω	1680 Ω

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NOVEL SHAPED-BEAM MICROSTRIP SLOT ARRAY SERIES FED BY STEPPED-IMPEDANCE LINE

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ABSTRACT: *A series-fed eight-slot microstrip array antenna operating at 3.5 GHz with a cosecant-squared shape beam is presented. The shaped radiation pattern is achieved by changing only the characteristic impedance of the series fed line between slots. The proposed antenna has a shaped-beam with elevation coverage of 35°, a gain of 10.86 dBi, and side lobe levels less than −19 dB. Since the slots and fed strip are fabricated on a single substrate, the antenna is easy to manufacture and low cost. Experimental results demonstrate the validity of this design.* © 2008 Wiley Periodicals, Inc. Microwave Opt Technol Lett 50: 2434–2437, 2008; Published online in Wiley InterScience (www.interscience.wiley.com). DOI 10.1002/mop.23662

Key words: *series-fed array antenna; shaped beam; microstrip slot antenna*

1. INTRODUCTION

In wireless communication systems, antennas with shaped radiation patterns have been widely used for better power managements. Shaped radiation patterns are usually realized by parallel feeding arrays, where the required patterns are shaped by controlling the feeding amplitudes and phases of array elements or by tuning the intervals between elements and the phases of elements [1–5]. Parallel-fed arrays can be easily designed but it may consume more energy in its parallel feed lines, and then decrease the efficiency of the array. Moreover, the feeding network and the antenna must be designed and manufactured separately, which would increase the cost of the antenna. Besides, series-fed arrays have been also reported to achieve shaped beams [6–8], and in those articles the feeding points or the structures of radiation elements were adjusted to shape the radiation beams. Nevertheless, those methods are mostly based on the equiv-