

A PLL with 30% Jitter Reduction Using Separate Regulators

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Abstract

A PLL using separate regulators to reject the supply noise is proposed in this paper. Two regulators, REG1 and REG2, are used to prevent the supply noise from the charge pump (CP) and the voltage-controlled oscillator (VCO), respectively. By using separate regulators, the area and the power consumption of the regulator can be reduced. Moreover, the jitter of the proposed PLL is proven on silicon to be less sensitive to the supply noise. The proposed PLL is fabricated using a typical 0.35 μm 2P4M CMOS process. The peak-to-peak jitter (P2P jitter) of the proposed PLL is measured to be 81.8 ps at 80 MHz when a 250 mVrms supply noise is added. By contrast, the P2P jitter is measured to be 118.2 ps without the two regulators when the same supply noise is coupled.

Key words: PLL, peak-to-peak jitter, supply noise, regulator, charge pump

1 Introduction

Most mixed-signal circuits need a PLL (phase-locked loop) to generate a stable clock for ADC, DAC or digital circuits. For example, the receiver of the DVB-T digital television requires an ADC with a sampling clock of 30 MHz for the baseband bandwidth of 8 MHz [1]. The jitter of the PLL is considered as a critical factor for the correct data transformation in these applications. Many prior efforts to discuss the reasons as well as the rejection methods of the PLL jitter have been announced, [2], [3]. The main source causing the PLL jitter is the supply noise and the substrate noise [2]. Several prior works proposed a variety of methods to reduce the supply noise in order to

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suppress the jitter. [3]-[5], [12], [13]. Two methods are widely used for reducing the PLL jitter caused by supply noise : differential topology [3] and power regulation [4]. For example, Maneatis proposed the self-biased techniques with differential structure to achieve a PLL with low jitter, and fixed damping factor [5]. Kaenel proposed a PLL using a high performance regulator to suppress the supply noise. However, the high performance regulator has the penalty of large chip area. Besides, the high performance regulator intrinsically causes design complexity due to the frequency compensation topologies [6]. By contrast, this paper proposes a PLL using separate regulated power supplies for the charge pump and the VCO, respectively. By using separate regulators, the area and power cost would be reduced. The physical measurements on silicon verifies that the P2P jitter is merely 81.8 ps at 80 MHz with the presence of a 250 mVrms supply noise.

2 PLL Using Separate Regulators

In order to remove the effects of the supply noise, a single voltage regulator for the charge pump (CP) and the voltage-controlled oscillator (VCO) could be used. The load regulation of a traditional regulator is proportional to the dimension of the pass transistor of the regulator, as shown in Eqn. (1).

$$\text{load regulation} = \frac{\Delta V_{\text{out}}}{\Delta I_{\text{out}}} = R_{\text{out}} = \frac{R_{\text{o-pass}}}{1 + A_{\text{OL}}\beta} = \frac{1}{g_{\text{m}_{\text{o-pass}}}(1 + A_{\text{OL}}\beta)}, \quad (1)$$

where $R_{\text{o-pass}} (= 1/g_{\text{m}_{\text{o-pass}}})$ denotes the output resistor of the pass transistor, A_{OL} denotes the open loop gain, and β is the feedback factor. To reject the severe vibration at VCO, it requires efficient load regulation by the regulator. According to Eqn. (1), the excellent load regulation needs large $g_{\text{m}_{\text{o-pass}}}$ and A_{OL} . It implies that a large pass MOS transistor is a must. Moreover, by connecting the VCO and the CP, the noise resulted from the vibration VCO might be coupled to the CP, which is supposed to provide a stable driving current. Such a coupling for the VCO and CP is undesirable, because the supply noise will deteriorate the output jitter through the CP.

Fig. 1 shows the block diagram of the proposed PLL, which is composed of a 2nd order charge pump PLL and the proposed dual regulators. The transfer function of each block is also revealed in Fig. 1. Notably, V_{n1} and V_{n2} denote the supply noise directly injected into the CP and VCO of the traditional 2nd order charge pump PLL, respectively. $V_{\text{n1}'}$ and $V_{\text{n2}'}$ denote the supply noise coupled to the dual regulators of the proposed dual regulation PLL, respectively.

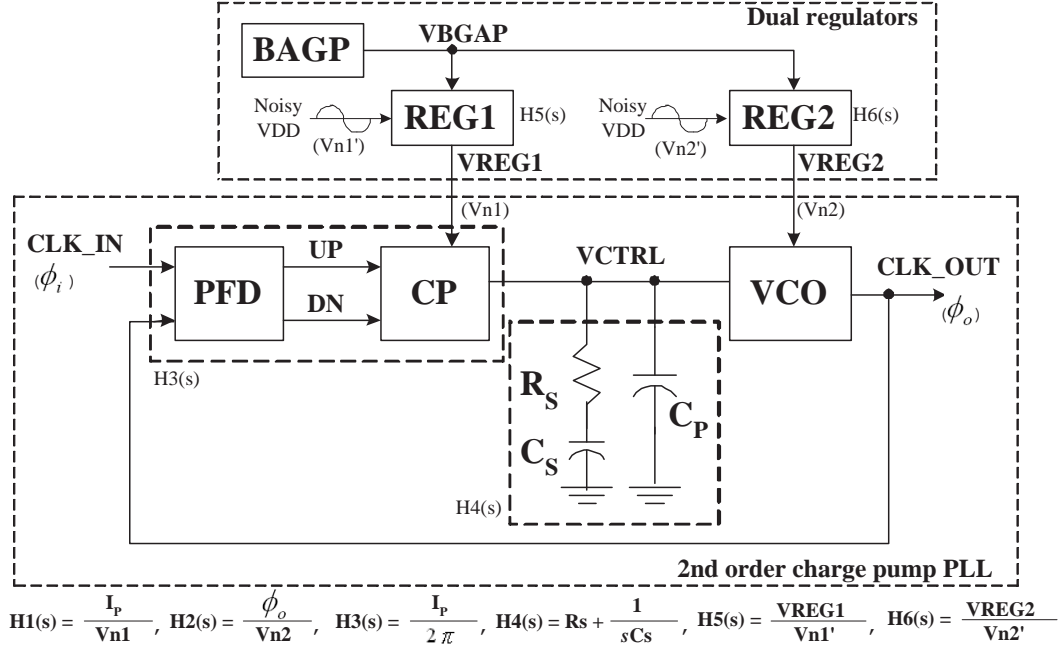


Fig. 1. The block diagram of the proposed PLL.

Regarding the 2nd order charge pump PLL without the dual regulators, the power supply of CP and VCO would be biased at VDD directly. Thus, the supply noise Vn1 and Vn2 would be fed into CP and VCO directly. According to the transfer function of each block shown in Fig. 1, the output phase in closed loop can be found to be

$$\phi_o = [(\phi_i - \phi_o) \cdot H3(s) + H1(s) \cdot V_{n1}] \cdot H4(s) \cdot \frac{K_{VCO}}{s} + H2(s) \cdot V_{n2}, \quad (2)$$

By setting $GH(s) = H3(s) \cdot H4(s) \cdot \frac{K_{VCO}}{s}$, the output phase can be derived to be

$$\phi_o = \left[\frac{GH(s)}{1 + GH(s)} \right] \cdot \phi_i + \left[\frac{H1(s) \cdot H4(s) \cdot \frac{K_{VCO}}{s}}{1 + GH(s)} \right] \cdot V_{n1} + \left[\frac{H2(s)}{1 + GH(s)} \right] \cdot V_{n2}, \quad (3)$$

The output phase ϕ_o is expressed as a function of the input phase ϕ_i , and the supply noise, Vn1 and Vn2. Referring to Eqn. (3), the low-frequency components of Vn1 would affect ϕ_o and the high-frequency components of Vn1 can be suppressed by the pole of H4(s). Intuitively, Vn1 is low-passed by the LF. By contrast, Vn2 would not be filtered by the LF and then contaminate the output phase ϕ_o directly.

In order to filter the supply noise, Vn1 and Vn2, and avoid the mentioned area penalty caused by the large pass transistor, the dual regulators are employed in the proposed design, as shown in Fig. 1. With the dual regulators, the

CP and VCO are powered by REG1 and REG2, respectively. Thus, the supply noise, $V_{n1'}$ and $V_{n2'}$, would be coupled to the dual regulators REG1 and REG2, respectively, and would not directly affect the CP and VCO. Similarly, the closed loop transfer function of the proposed PLL with dual regulators will be

$$\phi_o = \left[\frac{GH(s)}{1 + GH(s)} \right] \cdot \phi_i + \left[\frac{H1(s) \cdot H4(s) \cdot \frac{K_{VCO}}{s}}{1 + GH(s)} \right] \cdot H5(s) \cdot V_{n1'} + \left[\frac{H2(s)}{1 + GH(s)} \right] \cdot H6(s) \cdot V_{n2'}, \quad (4)$$

where $H5(s)$ and $H6(s)$ denote the frequency response of REG1 and REG2, respectively. $H5(s)$ and $H6(s)$ are the major difference between Eqn. (3) and (4). Moreover, $H5(s)$ and $H6(s)$ would suppress the supply noise $V_{n1'}$ and $V_{n2'}$, respectively. Design of the regulators will be discussed in the following subsection.

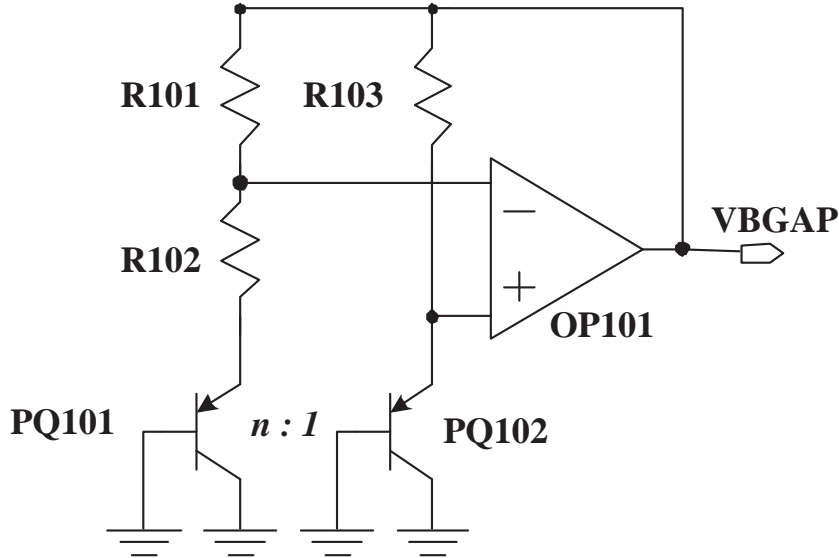


Fig. 2. The bandgap bias.

2.1 Submodules of the proposed PLL

Regulators (REG1, REG2): To reduce the supply noise, the bandgap bias must be insensitive to the supply voltage. Referring to Fig. 2, the output voltage VBGAP of the bandgap bias can be expressed as the following equation.

$$V_{BGAP} = V_{EB, PQ101} + (V_T \ln n) \left(1 + \frac{R101}{R102} \right), \quad (5)$$

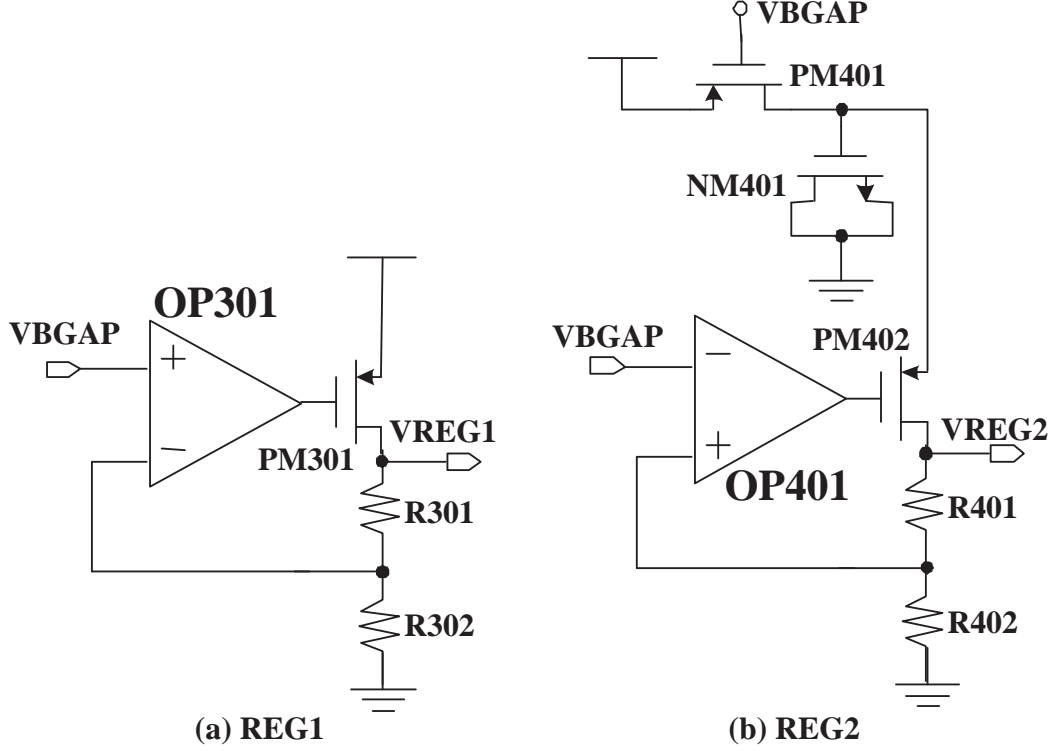


Fig. 3. Schematic of REG1 and REG2.

where $V_{EB,PQ101}$ is the emitter-base voltage of PQ101, V_T is the thermal voltage, and n is the emitter area ratio of PQ101 to PQ102. The supply voltage VDD is not included in the expression. Thus, VBGAP is insensitive to VDD.

As mentioned in the previous section, $H5(s)$ of REG1 must suppress the low-frequency noise. In order to filter the low-frequency supply noise, a step-down regulator REG1 can be employed, as shown in Fig. 3 (a). REG1 is a regulator which is composed of an error amplifier OP301, a pass transistor PM301, and a resistive feedback network R301 and R302. Because $R_s = 50 \text{ K}\Omega$ and $C_s = 5 \text{ pF}$ are chosen, the LF is treated as a low-pass filter with a pole at 4 MHz. Thus, REG1 must filter the supply noise with frequency below 4 MHz. This requirement can be achieved easily, since the step-down regulator can inherently generate a stable output voltage at low frequencies.

Fig. 3 (b) shows the schematic of REG2, which is composed of a step-down regulator (including the error amplifier OP401, the pass transistor PM402 and the resistive feedback network R401 and R402,) and a low-pass filter PM401 and NM401. According to the previous discussion, $H6(s)$ of REG2 should compress both the low-frequency component and the high-frequency component of supply noise V_{n2} . Because the step-down regulator can only suppress the low-frequency supply noise, a low pass filter is employed at the source of the pass transistor PM402 such that the high-frequency and low-frequency noise components can be filtered. Notably, the MOS resistor PM401 and the MOS

capacitor NM401 are used to replace traditional R-C LPF configuration to reduce the area overhead. The gate of PM401 is biased at VBGAP but not biased at GND directly for possessing a high resistance.

In order to sustain the stable output voltage of REG1 and REG2, the loop bandwidth of the regulators must be large enough. The step-down regulators possess three poles, which are the dominant pole contributed by the error amplifier, the gate pole contributed by the parasitic capacitor at the gate of the pass transistor, and the loading pole contributed by the loading current. Because REG1 and REG2 cooperate with the low-pass filters, the output current is smoothed. Thus, the loading pole can be ignored. Besides, the gate pole can also be ignored because the pass transistors have reasonable size of $100 \mu\text{m}/5 \mu\text{m}$ and $100 \mu\text{m}/2 \mu\text{m}$ at PM301 and PM401, respectively. Thus, the loop bandwidth of the regulators would be determined by the performance of the error amplifiers, OP301 and OP401. The error amplifier OP301, and OP401 employ the 2-stage operational amplifier which use PMOS transistors as the input transistors in the first differential stage. The gain and the bandwidth of the operational amplifier is simulated to be 89.97 dB and 8.78 MHz, respectively. The proposed regulators possess a 26.2 dB PSRR at 80 MHz based on simulation. Besides, the regulators cause voltage drops of 0.8 V for the CP and the VCO.

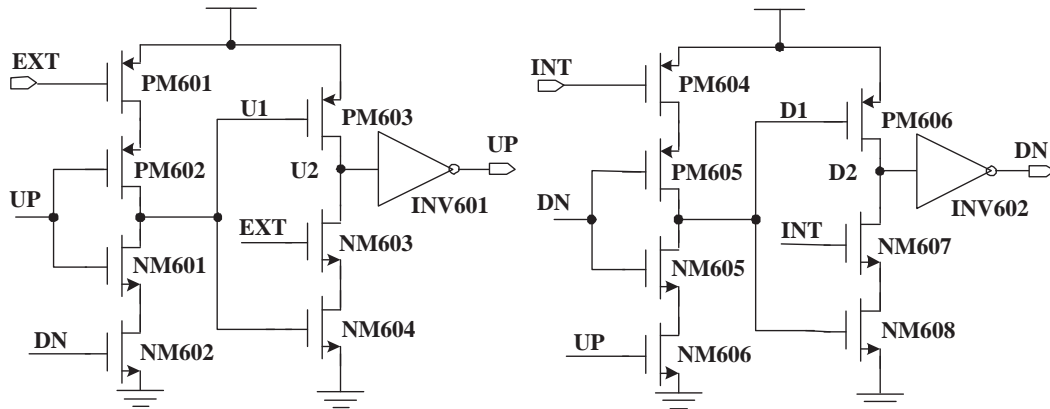


Fig. 4. The zero deadzone PFD.

PFD: The deadzone is the most important parameter for PFD due to that it is the major source of the PLL phase error. The deadzone introduces the phase jitter when the control voltage, VCTRL, is within the deadzone. A lot of different PFDs have been proposed to resolve the problem of long delay, limited operating frequency, or long deadzone, [7], [8]. The most extensive PFDs are the dynamic PFDs which attain the advantages of high speed and zero deadzone. The PFD shown in Fig. 4 is used in the proposed PLL. The node EXT and INT refer to the signal CLK_IN and CLK_OUT, respectively. The two-stage structure carries out the precharge function such that high speed is achieved. The feedback control signal for PM602 and NM601 for UP (similarly,

PM605 and NM605 for DN) makes the zero deadzone possible. Moreover, the drawback of a short-circuit current from VDD to GND is eliminated because PM602 and NM601 for UP (similarly, PM605 and NM605 for DN) do not turn on at the same time [8].

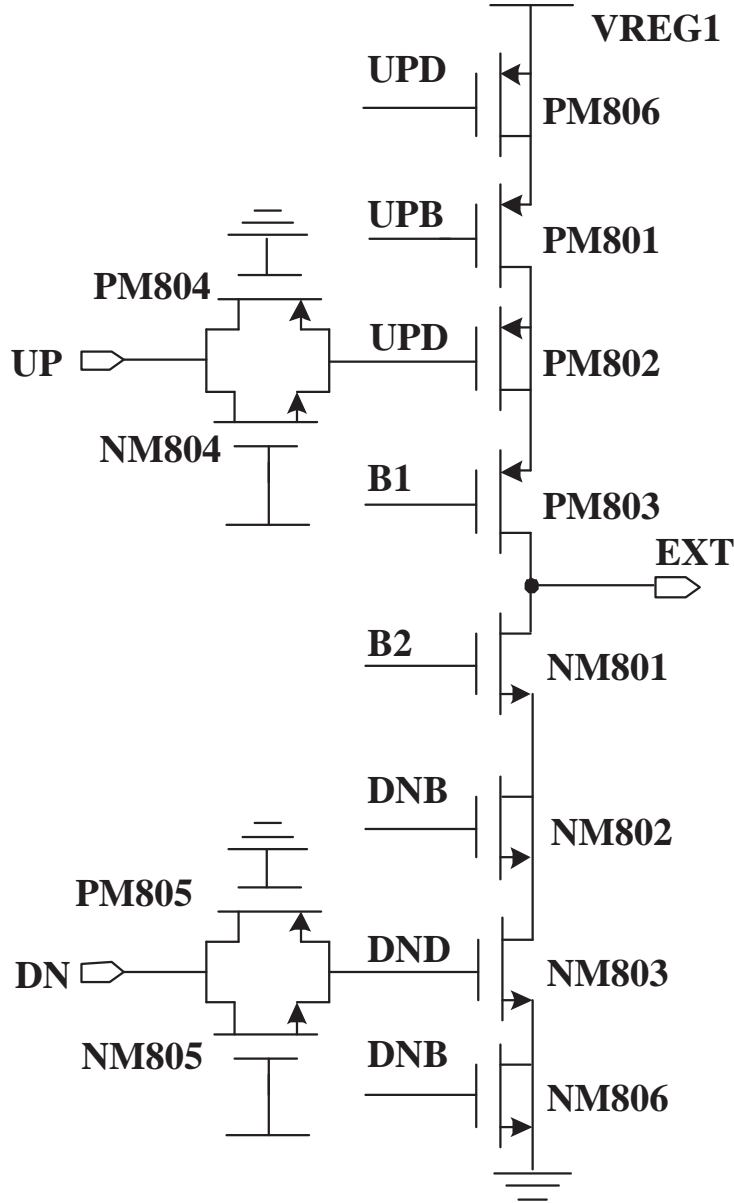


Fig. 5. Schematic of the charge pump.

CP: REG1 is in charge of the noise rejection for CP. Besides, the switching speed of CP is another important source for the PLL jitter. Thus, a switch is placed in the source of the mirrored MOS transistors for the speed consideration in Fig. 5 [9], where PM801 (NM803) is the switch of current, PM803 (NM801) is the mirrored current source, PM802 and PM806 (NM802 and NM806) are for the charge injection reduction, PM804 and NM804 (PM805

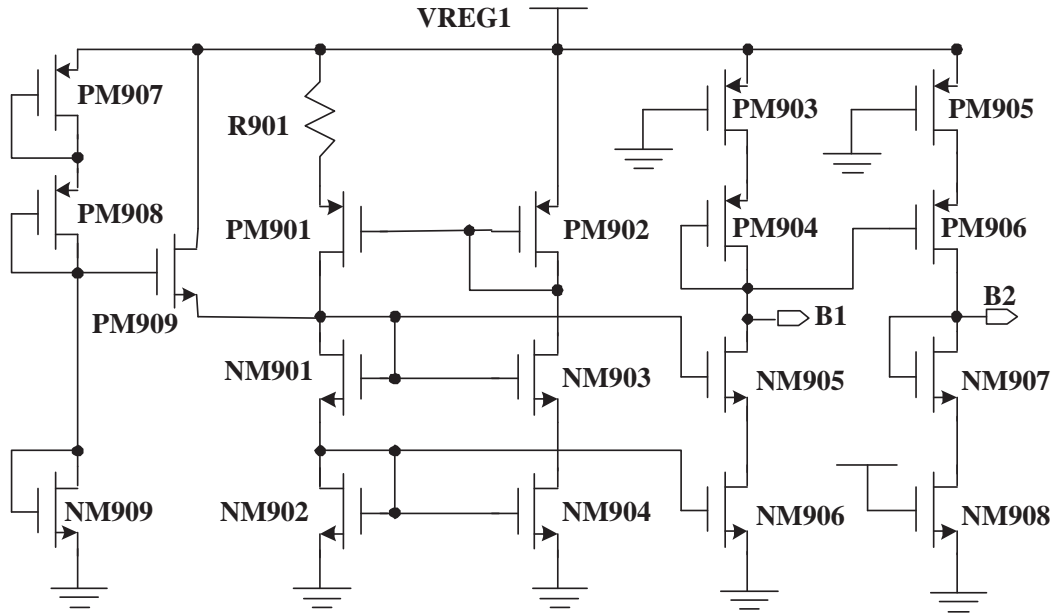


Fig. 6. The bias circuit of CP.

and NM805) consist of a dummy delay element for eliminating the skew of the control signal, and UPB and DNB are the inversions of UP and DN, respectively. Thus, the control signals, UPD, UPB, DNB, and DND, can be activated without any time delay. Notably, the output current of the bias generator for CP shown in Fig. 6 is ideally independent of the supply voltage.

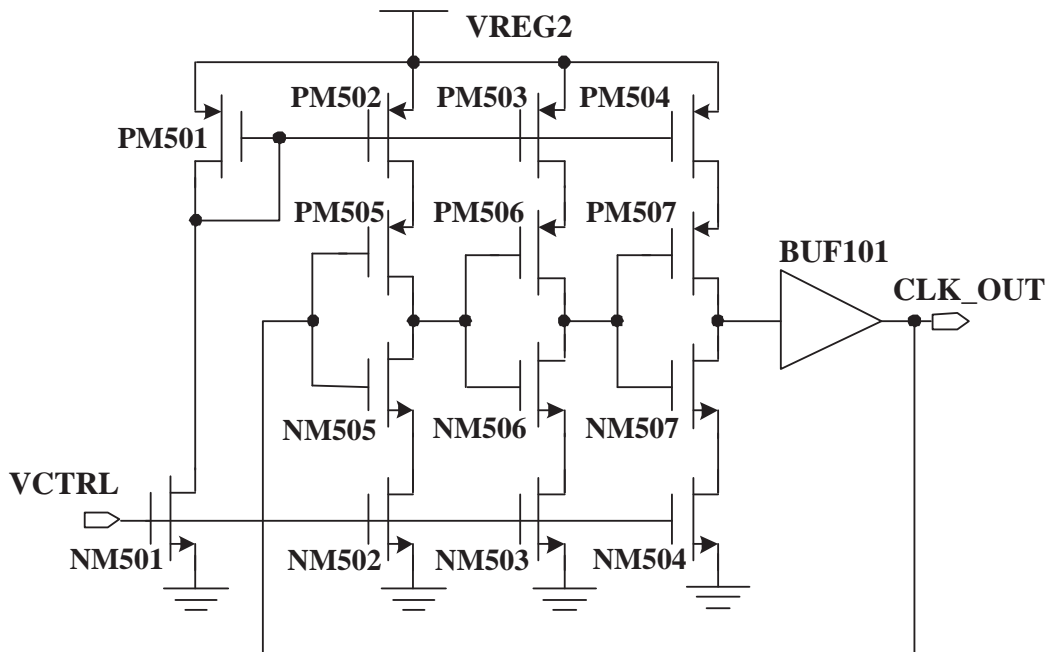


Fig. 7. The current-starved VCO.

VCO: The current-starved inverters are used to construct the VCO, as shown in Fig. 7. With the current-starved structure, the supply noise would contaminate the output phase. Referring to Eqn. (6), the output frequency can be assumed to be in terms of the RC delay and n denoting the number of the inverter stages. C_{tot} denotes the total parasitic capacitance including C_{wire} (wire parasitic capacitor), and C_{DB} (Drain-to-Bulk capacitor). For simplifying the analysis, C_{DB} is assumed to be a constant regardless of the operation mode of the transistors. Moreover, the resistance of the channel of each stage (R) could be estimated as the reciprocal of the transconductance of the MOS. With $\phi_o = \frac{\partial f_o}{\partial t}$, the supply noise would change the V_{GS} of the PMOS and further affect the output frequency and output phase.

$$f_o \propto \frac{1}{n \cdot R \cdot C_{\text{tot}}} = \frac{g_m}{n \cdot C_{\text{tot}}} = \frac{\mu C_{\text{ox}} \left(\frac{W}{L}\right) (V_{\text{GS}} - V_{\text{TH}})}{n \cdot C_{\text{tot}}}, \quad (6)$$

where V_{TH} denotes the threshold voltage. The serious problem of supply noise coupled in the current-starved VCO will be resolved by REG2. Besides, the output buffer is added to maintain the gain of VCO when a large capacitive load is present.

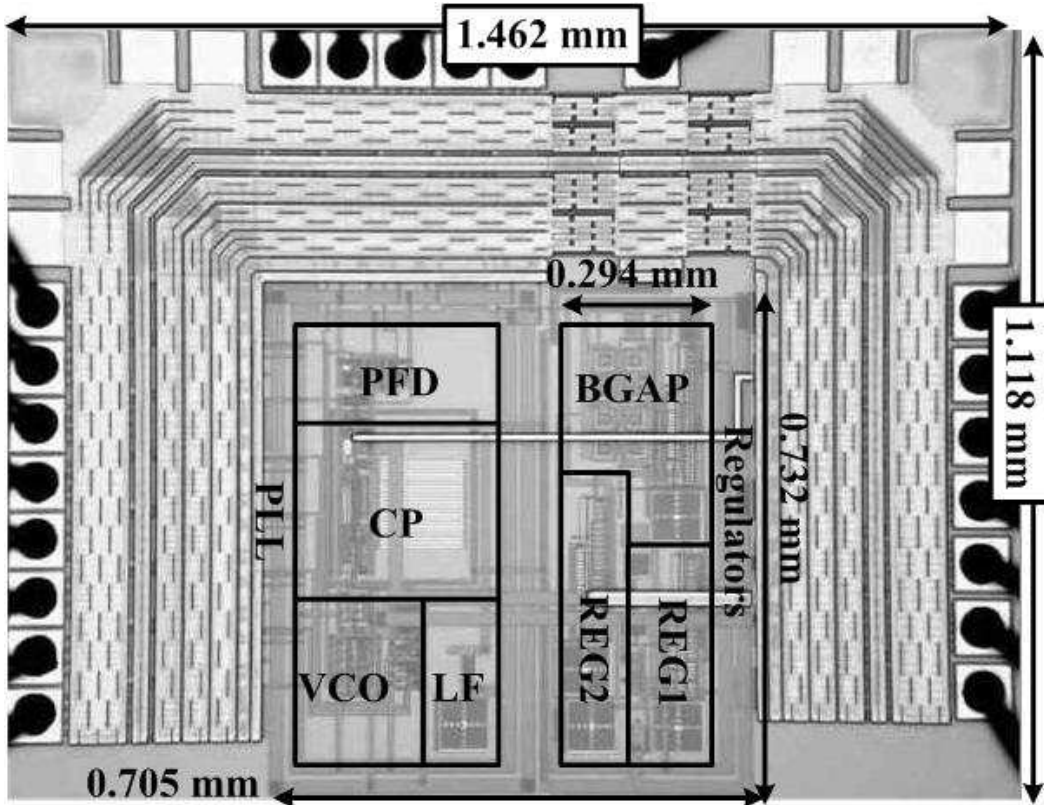


Fig. 8. The die-photo of the proposed PLL.

3 Implementation and Measurement

A typical $0.35\ \mu\text{m}$ 2P4M CMOS process is adopted to carry out the proposed PLL design. The die photo of the proposed PLL is shown in Fig. 8 where the core area is $705\ \mu\text{m} \times 732\ \mu\text{m}$. The total area including the PADS is $1.118\ \text{mm} \times 1.462\ \text{mm}$. In order to guarantee the functionality of the power regulators addressed in Section 2, the guard ring to reject the substrate noise from PLL to regulators must be added between the REG1, REG2 and the PLL.

The PSRR of the regulator is simulated to be 26.2 dB. Three 10 mV sinusoidal waves with 100 Hz, 100 KHz, and 80 MHz frequency, respectively, are coupled at the power supply to be the supply noise. With this dirty power supply, the simulated P2P jitter is 93.777 ps at the worst case simulation corner of SS model. The power consumption of the proposed PLL is simulated to be 15.857 mW at 80 MHz operating frequency.

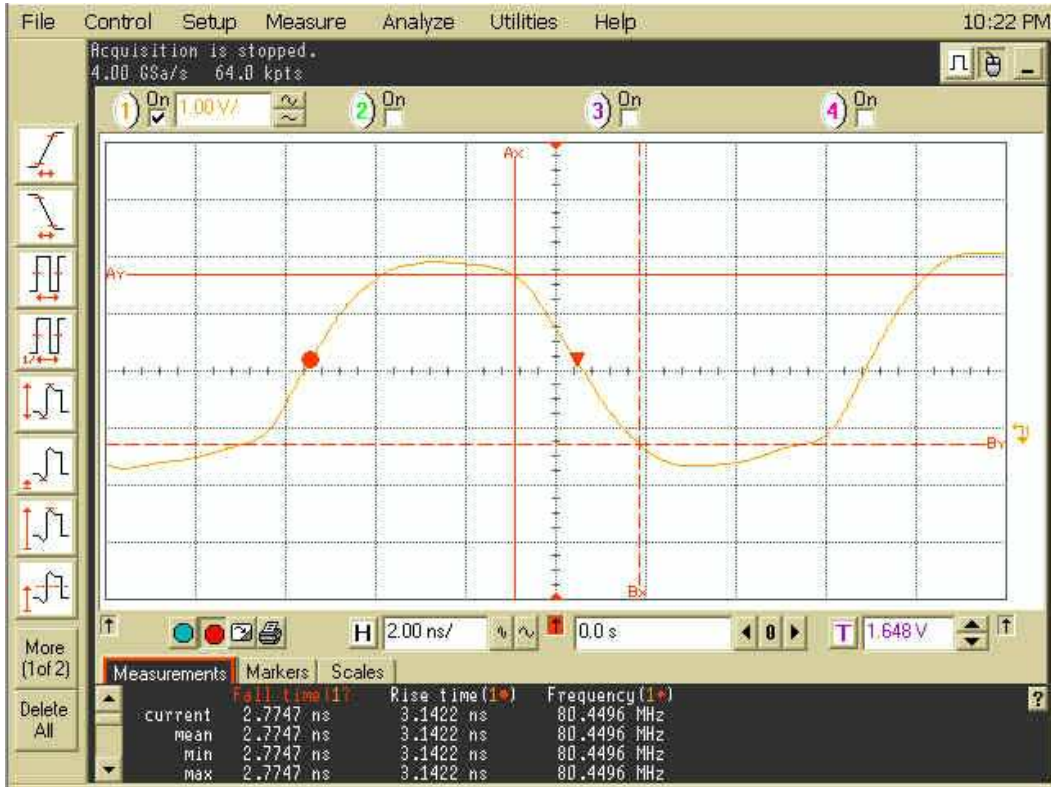


Fig. 9. The measured output waveform of the proposed PLL at 80 MHz and a 8 pF load from the probe.

The measurement environment of the PLL chip is set up on a PCB board. The quartz oscillator for the reference clock is HO-12B of HOSONIC ELECTRONIC CO., LTD. The power supplier is GW GPC-3030D. Agilent Infiniium Oscilloscope, 600 MHz, 4GSa/s, is employed in recording the PLL jitter of the

chip. The output waveform is 80 MHz, as shown in Fig. 9. The rise time and fall time are 3.1422 ns and 2.7747 ns, respectively. The equivalent load capacitance of the probe is 8 pF.

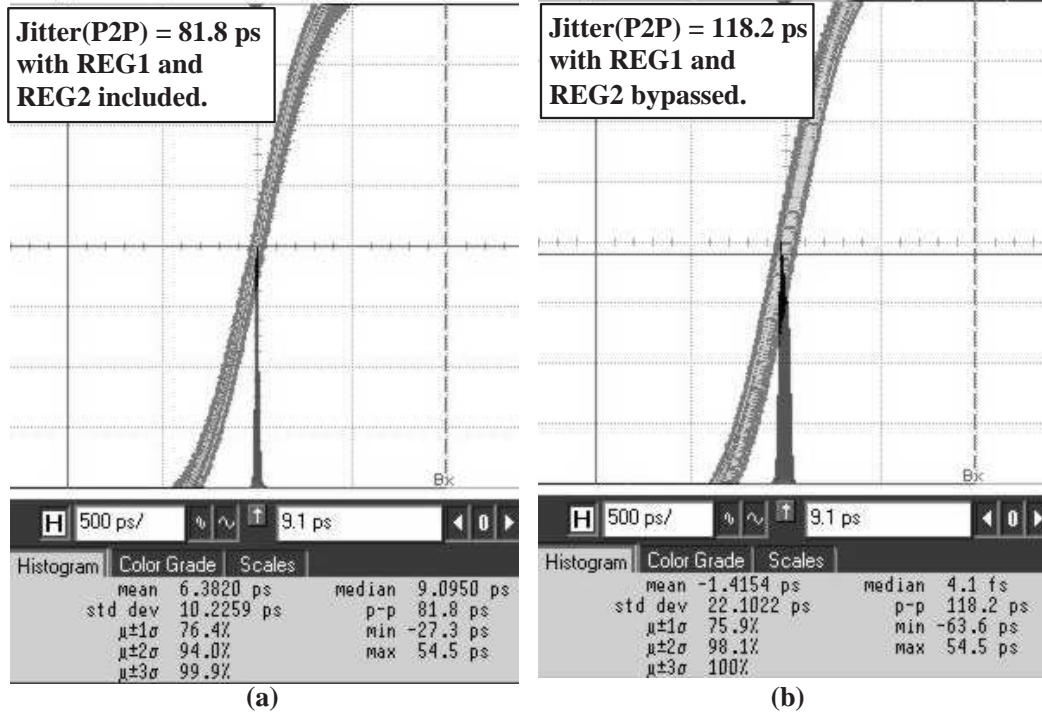


Fig. 10. The measurement jitter histogram of the proposed PLL with the 250 mVrms supply noise. (a) The supply noise is provided to the dual regulators. (b) The supply noise is coupled directly to the CP and the VCO.

Fig. 10 shows the measured jitter histograms in different conditions. The supply noise of 250 mVrms generated by Agilent 33250A is added to the proposed PLL with the regulators, REG1 and REG2. The measured P2P jitter is 81.8 ps, as shown in Fig. 10 (a). This measured P2P jitter is in the range of the predicted value of 93.777 ps by the simulation at the worst case. By contrast, when the 250 mVrms noise is coupled to the digital voltage supply node of the CP and the VCO, and the two regulators (REG1 and REG2) are bypassed, the P2P jitter is measured to be 118.2 ps, as shown in Fig. 10 (b). The measured jitter of the proposed PLL with the dual regulators is suppressed more than 30% than that without the dual regulators. It shows that the method of using two regulators can reduce the supply noise that affects PLL's output jitter. Besides, the P2P jitter is measured to be 72.7 ps when no supply noise is coupled to the dual regulators or to the CP and VCO directly. The total power consumption of the proposed PLL is 78 mW at 80 MHz. Notably, the measured power consumption includes the power due to the I/O PADS such that the measured power consumption is larger than that based on simulation.

	ours	[5]	[11]
CMOS process (S)	0.35 μm	0.5 μm	0.35 μm
Supply Voltage (V_{sp})	3.3 V	3.3 V	3.3 V
Power consumption (P @ f)	78 mW @ 80 MHz	9.24 mW @ 550 MHz ^b	200 mW @ 125 MHz ^b
FOM1 [‡]	0.731	0.006	1.199
P2P jitter	81.8 ps @ 250 mVrms supply noise	144 ps @ 500 mV/ 1MHz square wave supply noise	222 ps @ N/A
Core area (A)	0.516 mm ²	1.91 mm ²	2.89 mm ²
FOM2 [‡]	4.21	7.64	23.59
Topologies	Dual regulators	Self-biased & differential structure	Time- constant calibration

[‡] : FOM1 = $P/(fS^2V_{\text{sp}}^2)$, FOM2 = $A/(S^2)$, where S is the feature size of the process.

^b : Assume that the power consumption is measured at the maximum operating frequency.

Table 1

Performance comparison of the proposed PLL and prior works.

Besides, a performance comparison of the proposed design on silicon with several prior PLLs are summarized in Table 1. Notably, the P2P jitter of the proposed design is 43% better than that of Maneatis’s design [5]. It seems to take the penalty of 8.44 times of power consumption. However, the power consumption of 78 mW of the proposed design includes the excess power consumption of the PADs. Thus, the penalty of power consumption is not really serious. Two FOM (figure of merits) are given to normalize the performance of those works. FOM1 is the normalization for the power consumption, as shown in follows.

$$\text{FOM1} = \frac{P}{f \cdot C \cdot V_{\text{sp}}^2} = \frac{P}{f \cdot S^2 \cdot V_{\text{sp}}^2}, \quad (7)$$

where C is to indicate the capacitor’s area which can be assumed to be proportional to the square of the feature size of the corresponding process (S). With the normalization, the PLL using self-biased and differential structure consumes the least power. However, the jitter performance is not good enough. On the other hand, FOM2 ($= \frac{A}{S^2}$) is to compare the area with respect to the feature size of the corresponding CMOS process. The normalized area of the proposed PLL is revealed to be better than that of the other works.

4 Conclusion

We have proposed a PLL with two regulators to isolate the supply noise for CP and VCO, respectively. The measurement results verify that the proposed design can reject the supply noise into the output jitter of the PLL. The jitter can be reduced by more than 30 % by the proposed design according to the measurement on silicon.

Acknowledgement

This research was partially supported by National Science Council under grant NSC 96-2923-E-110-001-MY2 and National Health Research Institutes, under grant NHRI-EX97-9732EI. Furthermore, the authors would like to express their deepest gratefulness to CIC (Chip Implementation Center) of NARL (National Applied Research Laboratories), Taiwan, for their thoughtful chip fabrication service. The authors also like to thank “Aim for Top University Plan” project of NSYSU and Ministry of Education, Taiwan, for partially supporting the research.

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