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A HIGH-SFDR DIRECT DIGITAL FREQUENCY SYNTHESIZER WITH EMBEDDED ERROR-COMPENSATION CMOS OTP ROM FOR WIRELESS RECEIVERS

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ABSTRACT: *A direct digital frequency synthesizer (DDFS) using on-chip CMOS one-time programmable read-only memory (OTP ROM) is presented. A straight-line approximation algorithm for sinusoid with compensation is adopted such that the accuracy could be maintained and the cost is reduced. Most important of all, a CMOS OTP ROM is used as a look-up ROM table, which is implemented by a typical logic CMOS process. Therefore, the proposed DDFS can be integrated in any CMOS-based front-end circuit for wireless communication systems. The proposed DDFS design is fully implemented using a typical 1P6M 0.18 μm CMOS process. It has a 12-bit amplitude resolution with 86.89 dB spurious free dynamic range using a small ROM size of 256 bits.* © 2009 Wiley Periodicals, Inc. Microwave Opt Technol Lett 51: 1695–1699, 2009; Published online in Wiley InterScience (www.interscience.wiley.com). DOI 10.1002/mop.24422

Key words: *frequency synthesizer; DDFS; one-time programmable; OTP; wireless communication; straight-line approximation*

1. INTRODUCTION

The frequency synthesizer is an important part of a communication system, particularly in the receiver front-end, where sinusoidal signals are required to down-convert a high-frequency-modulated input signal to an intermediate frequency (IF) band, which will then be demodulated into a baseband signal [1]. Phase-locked loops (PLL) were widely used for frequency synthesis traditionally. As the frequency is getting higher, the power consumption becomes a serious problem in a portable communication device. When compared with PLL, DDFS has faster frequency switching, higher resolution, better spectral purity, lower phase noise, and continuous-phase frequency switching. Moreover, DDFS allows direct phase and frequency modulation in the digital domain [2].

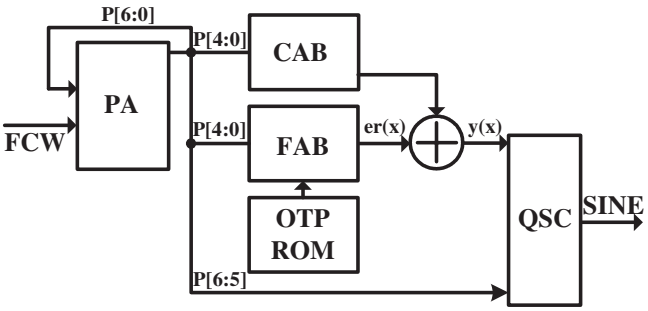


Figure 1 Block diagram of the proposed DDFS

In prior DDFS researches, ROM-based (or namely table look-up) methods have been widely studied, for example, [3–5]. The conventional nonvolatile ROM such as EPROM, EEPROM, and flash EEPROM, are manufactured with a special process. As the SOC evolving lately, the programmable non-volatile memory manufactured with typical logic CMOS process is strongly needed to physically integrate the DDFS and ROM into a single chip.

Many researches for OTP ROMs have been proposed. Most of them used either fusing or antifusing technology [6], for example, polyfusing, oxide-nitride-oxide (ONO) [7], and metal-oxide-metal (MOM) [8, 9]. Polyfusing is not adaptable because of process changing, while the ONO and MOM require additional process steps. Therefore, none of them is suitable for CMOS-based SOC fabricated by a typical logic process. With the development of deep-submicron technologies, the gate oxide of transistors becomes very thin which makes break down thereof very much easy. The transistor can be punched-through (antifused) without damaging other circuits in a neighborhood region. Then, OTP ROM realized by logic CMOS processes without any postprocess is feasible. This kind of OTP ROM can be used to increase the flexibility and calibratablity of an ASIC or SOC after chip fabrication. In this article, we propose a DDFS using the straight-line approximation for quadrant sinusoid. Most important of all, the error compensation is carried out by a COMS OTP look-up ROM table to save the hardware cost and justify the SOC feasibility.

2. THE PROPOSED DDFS DESIGN

A perfect sinusoidal wave is cyclic and symmetrical. It could be reconstructed with a quadrant waveform. The straight line approximation is deemed as one of the easiest algorithms to realize with digital circuitry. The classic straight line approximation approximates the quadrant sinusoid with n segment straight lines by choosing the closest slope m_i and intercept b_i. However, it will increase the number of processing units to design a high accuracy DDFS in the classic way, if n becomes very large.

TABLE 1 The Coefficients in CAB Part

i	m_i	b_i	x
0	3	3	0–11
1	2	14	12–21
2	1	34	22–29
3	1	32	30–31

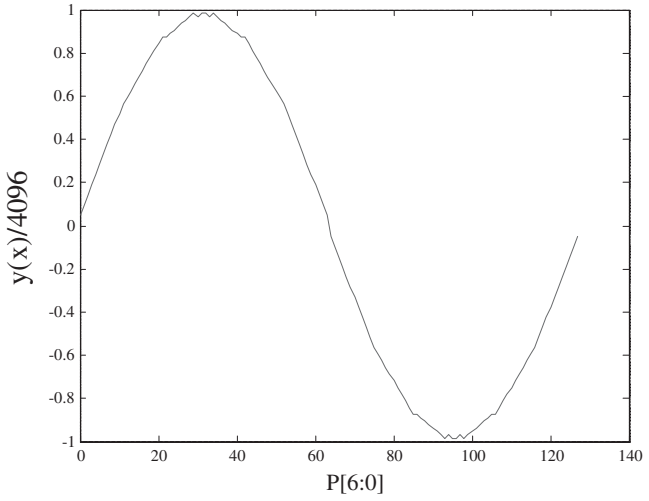


Figure 2 The sinusoid approximation without error compensation

The proposed DDFS is divided in two parts, that is, coarse approximation block (CAB) and fine approximation block (FAB). The low accuracy approximate waveform will be calculated in CAB part using the straight line approximation. Then, the error compensation will be carried out by looking up an OTP ROM table on the same chip to derive the waveform with a high resolution in FAB. The sinusoidal wave can be expressed as follows.

$$y(x) = \begin{cases} (m_0 x + b_0)2^k + er_0(x), & x_0 \le x < x_1 \\ (m_1 x + b_1)2^k + er_1(x), & x_1 \le x < x_2 \\ \vdots & \\ (m_{n-1} x + b_{n-1})2^k + er_{n-1}(x), & x_{n-1} \le x < x_n \end{cases}$$

where x is the output of the phase accumulator, whereas the m_i, b_i are the slope and intercept of each segment, respectively, $er_i(x)$ is the error value of x to compensate the coarse approximation, and k is the shift index for saving the number of multipliers.

2.1. DDFS Design

Figure 1 shows the block diagram of the proposed DDFS design. The phase accumulator (PA) translates the frequency control word (FCW) into control signals of the other function blocks, P[6:0].

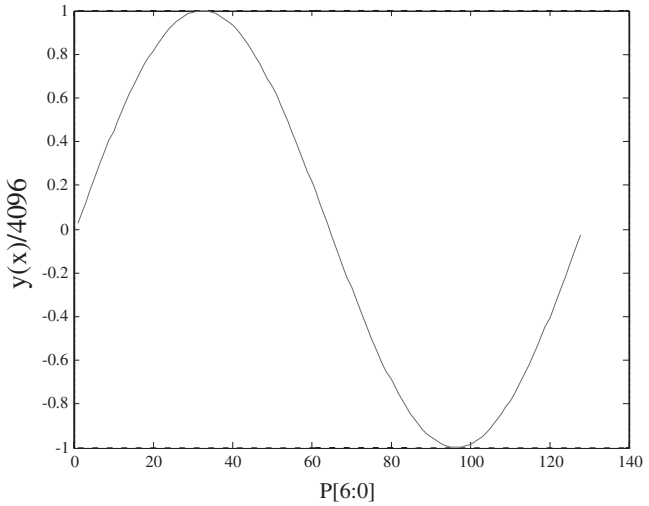


Figure 3 The sinusoid approximation with error compensation

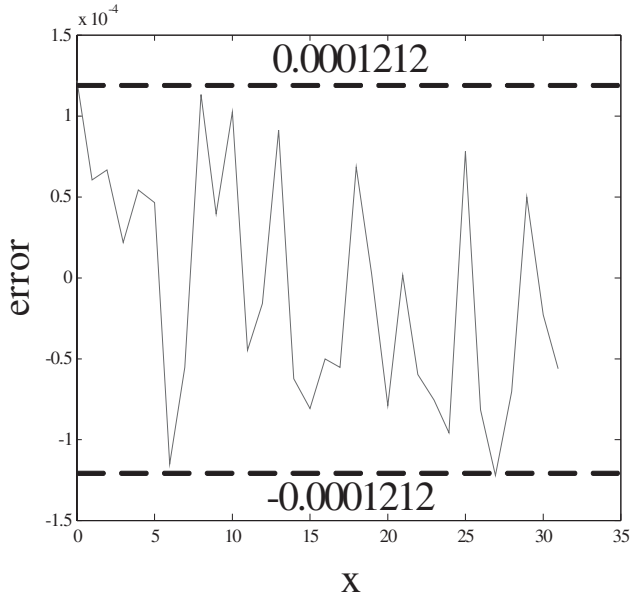


Figure 4 The error between the perfect waveform and the output waveform

Generally, the phase accumulator works like a counter, whose parameters are decided by FCW. Thus, the frequency of the output sinusoidal wave can be adjusted. The first two bits of PA output (i.e., P[6:5]) are used to reconstruct the complete digital sinusoidal waveform from the quadrant waveform in the quadrant state control (QSC) block. The other bits (P[4:0]) notify the CAB and FAB parts as the variable x to calculate the quadrant approximate waveform magnitude accordingly. The CAB calculates the straight line approximation of the target sinusoidal wave, whereas the FAB looks up the table stored in an OTP ROM to get the error compensation value, $er_i(x)$. The quadrant waveform, $y(x)$, will be calculated by adding the straight line approximation and error compensation value. The digital output, SINE, is the complete sinusoidal waveform approximation reconstructed by switching the states of the quadrant sinusoidal waveform in QSC.

The proposed DDFS has an amplitude resolution of 12 bits. To reduce the hardware cost of the CAB and the FAB, the amplitude

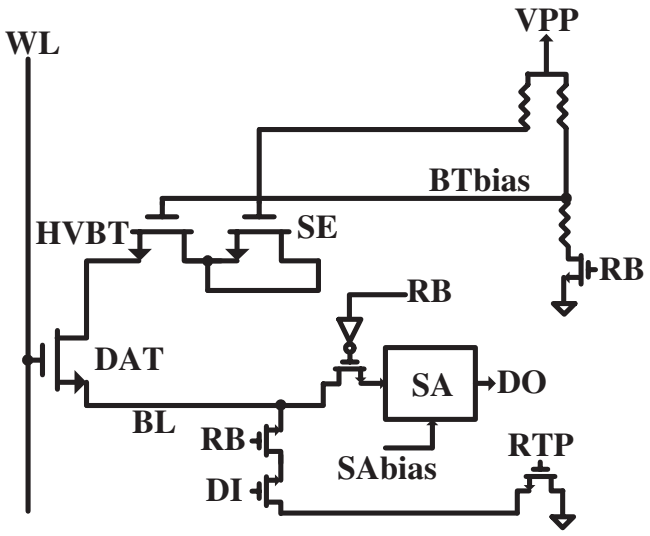


Figure 5 The OTP ROM cell

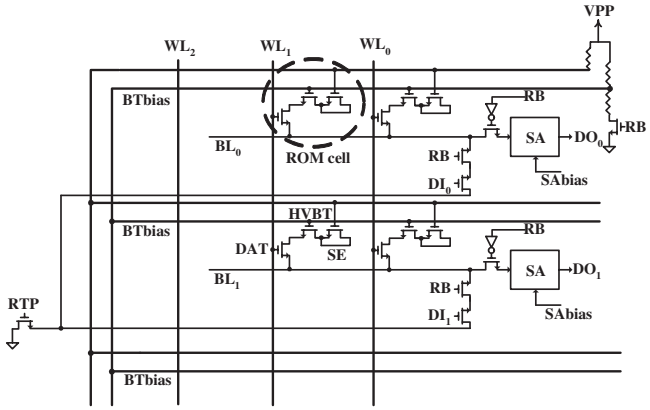
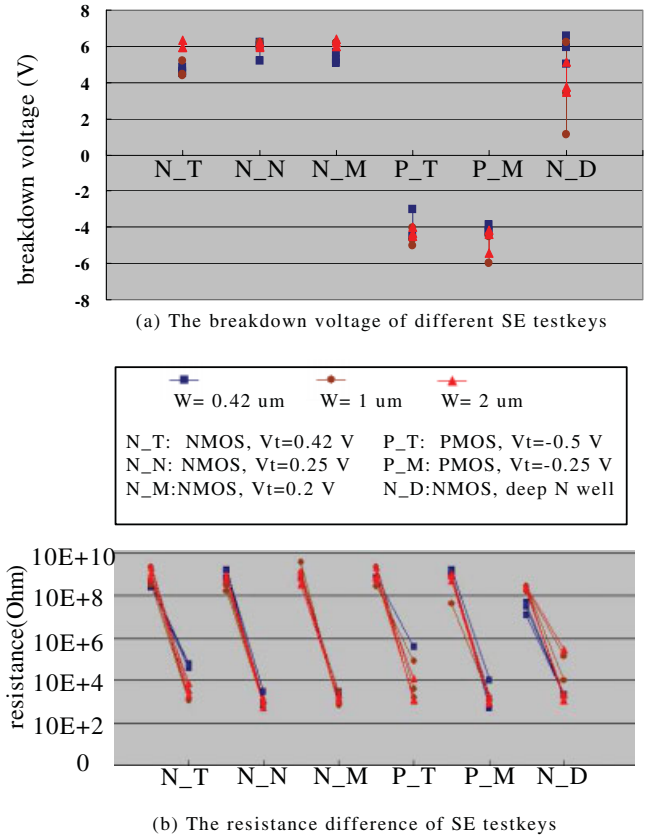


Figure 6 The OTP ROM array

resolution of CAB is six bits, such that $k = 6$ is chosen. Besides, the four segments of straight line can approximate the quadrant waveform almost as good as the five segments of straight line by thorough MATLAB simulations. The 4-segment approximation requires less amplitude resolution of CAB and certainly less hardware cost. Table 1 is a selected combination of coefficients in the CAB part after detailed simulations. By Table 1, the CAB part calculates the coarse approximation as shown in Figure 2. Then, we can derive each $er_i(x)$ by comparing it with the perfect sinusoidal waveform to generate the entries in the look-up ROM table. The simulation result after error compensation is shown in Figure 3. Figure 4 shows the error value between the output waveform



(a) The breakdown voltage of different SE testkeys

(b) The resistance difference of SE testkeys

Figure 7 OTP ROM test key measurement statistics. [Color figure can be viewed in the online issue, which is available at www.interscience.wiley.com]

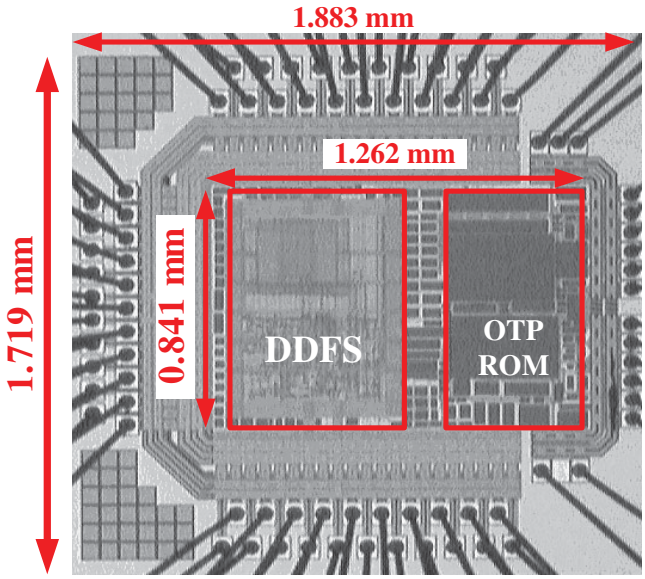


Figure 8 Die photo of the proposed DDFS design. [Color figure can be viewed in the online issue, which is available at www.interscience.wiley.com]

and the perfect waveform. Because the largest error value is about $0.000122 < 2^{12}$, the amplitude resolution of the DDFS is ensured to be 12 bits.

2.2. *CMOS OTP ROM*

Generally, there is a huge equivalent resistance between gate and bulk of a MOSFET fabricated by a standard CMOS process. If a high voltage is applied on the gate of the MOSFET, breakdown occurs to reduce the equivalent resistance sharply. This characteristic makes the standard CMOS process possible to realize OTP ROM. As long as we can control the programming time and voltage, we can write the data in the OTP ROM by "antifusing" the gate oxide correctly without damaging nearby circuitry.

Referring to Figure 5, the CMOS-based ROM cell is composed of three components: a storage element (SE), a high voltage blocking transistor (HVBT), and a data access transistor (DAT). In the programming mode, the target ROM cell will be selected by enabling word line (WL) and Data in (DI). The gate voltage of the SE in the target ROM cell will be pulled high by VPP to antifuse the gate oxide. HVBT will be turned on to relay the programming voltage to ground via DAT. The Read bar (RB), Data in (DI), and Ready to Program (RTP) will be pulled high to ensure the current path of target ROM cell in programming mode. In the mean time, HVBT of other ROM cells will be cut off

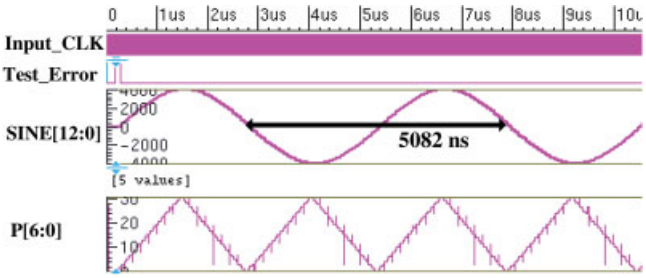


Figure 9 The postlayout simulation of a synthesized sinusoid. [Color figure can be viewed in the online issue, which is available at www.interscience.wiley.com]

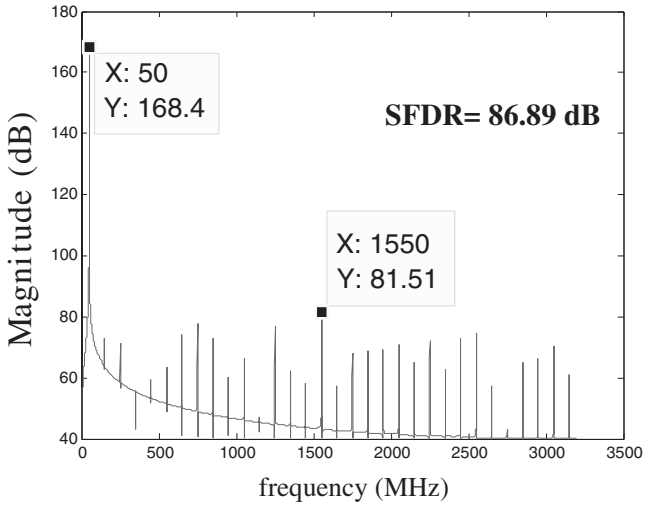


Figure 10 The SFDR

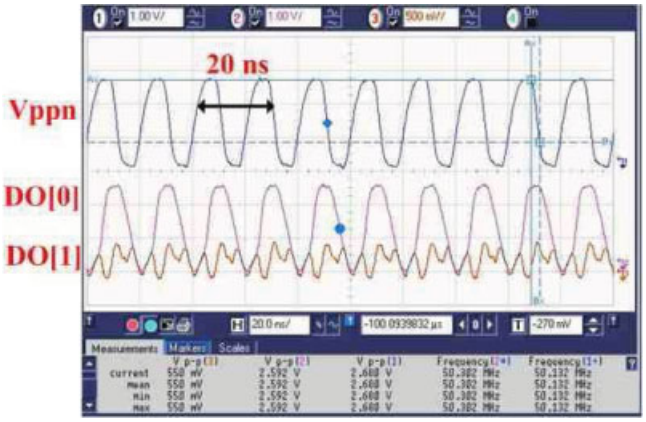


Figure 12 Partial readout measurement of the ROM array. [Color figure can be viewed in the online issue, which is available at www.interscience.wiley.com]

to prevent the programming voltage from damaging their data. In the reading mode, the binary digit stored in SE will be sensed from the current through the DAT, and differentiated by the sense amplifier (SA). In other words, the bit is stored in the SE in a resistance state, which can be sensed by a transimpedance amplification circuits. The OTP ROM cell array in the proposed design is shown in Figure 6.

To justify the feasibility of the CMOS OTP ROM, we have taped out several CMOS test keys with different SE designs by a typical 0.18 μm CMOS process. The design parameters of SE, including MOS types, sizes, and threshold voltages, have been fully tested. Each type of the SE test key has been supplied with high VPP until it is antifussed to find the most appropriate programming voltage and time. It is found that the most stable SE is the NMOS with 0.25 V threshold voltage (N N type), and the VPP voltage (programming voltage) is 6.5 V by the statistics shown in Figure 7(a). Notably, the size of the SE MOS does not really affect the VPP voltage. The resistance of SE before and after antifussing is measured on silicon to be about 100 KΩ and 100 MΩ, respectively, as shown in Figure 7(b), which justifies that it is suitable to construct an OTP ROM cell or array.

3. IMPLEMENTATION AND MEASUREMENT

TSMC (Taiwan Semiconductor Manufacturing Company) 0.18 μm 1P6M CMOS process is adopted to carry out the proposed DDFS design. The die photo of the proposed design is shown in Figure 8, the size of the chip core area is 841 μm $\times$ 1262 μm (1719 μm $\times$ 1883 μm with pads). Figure 9 shows the sinusoidal waveform. Test Error is the output of a build-in self test, indicating the correctness of the proposed design. The FFT result of the waveform is shown in Figure 10, where the spurious free dynamic range (SFDR) is 86.89 dB. The shmoo plot shown in Figure 11 reveals that the proposed DDFS chip can work correctly at the maximum frequency of 76 MHz with 2.2 V supply voltage. The measurement result of the QSC output, that is, SINE, is the same as the simulation result. Partial of the detailed readout measurement result of OTP ROM array is shown in Figure 12. The characteristics of the proposed design as well as the comparison with prior ROM-based DDFS designs are tabulated in Table 2. The proposed DDFS has the smallest ROM size and the best SFDR without sacrificing the amplitude resolution. Most important of all, the proposed DDFS is the only solution to integrate the digital DDFS with on-chip ROM on a single typical CMOS logic process.

Figure 11 The measurement shmoo plot of the proposed DDFS. [Color figure can be viewed in the online issue, which is available at www.interscience.wiley.com]

4. CONCLUSION

We have proposed a DDFS with error-compensation OTP ROM on a typical logic CMOS process. The straight line approximation for the quadrant sinusoid has been adopted in addition to the error compensation with small look-up ROM table without any loss of resolution, and the proposed DDFS design provides a better solution in terms of ROM size and SFDR.

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TABLE 2 The Comparison of the Proposed DDFS with Prior Works

	[3]	[4]	[10]	[5]	Proposed Design
Process (μm)	0.35	0.35	0.25	0.35	0.18
Amplitude resolution (bits)	12	9	12	12	12
Phase resolution (bits)	28	32	24	8	5
ROM size (bits)	448	368	N/A	3072	256
SFDR (dB)	84.2	55	80	78	86.89

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A SMALL PRINTED DUAL-BAND ANTENNA FOR MOBILE PHONES

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ABSTRACT: *A small printed antenna is proposed for dual-band applications. The antenna is patterned on the front of an 0.8-mm FR4 substrate to obtain a low-frequency resonance and a stub is patterned on the back of the substrate to obtain a high-frequency resonance. The antenna without ground plane is small (8 × 35 mm), and it is suitable to operate as an internal antenna. For S_{11} less than −6 dB, the antenna operates at 900 MHz with a bandwidth of 66 MHz, and at 1.8 GHz with a bandwidth of 130 MHz. Maximum radiation efficiencies were 52% at both 900 MHz and 1805 MHz.* © 2009 Wiley Periodicals, Inc.
Microwave Opt Technol Lett 51: 1699–1702, 2009; Published online in Wiley InterScience (www.interscience.wiley.com). DOI 10.1002/mop.24415

Key words: *inverted-F antenna; dual-band; printed antenna; mobile phone*

1. INTRODUCTION

Antennas for mobile phone are increasingly required to be smaller and to have low profile and high performance. The print circuit board (PCB) antenna is widely used for mobile devices due to its low profile and easy fabrication. A printed loop antenna mounted perpendicular to the top edge of the PCB has been proposed for GSM/DCS/PCS/UMTS operations [1]. A PCB multiband mobile phone antenna based on the folded planar inverted F antenna has been suggested for GSM (890–960 MHz) and DCS (1710–1880 MHz) bands [2]. A two-printed monopole slot antenna for multi-band mobile phone has also been proposed [3]. Quad-band antennas based on metamaterial theory have also been printed on PCBs [4]. However, most of these antennas are too large for use as the internal antenna of a mobile phone.

In this article, we propose an electrically small dual-band PCB antenna for mobile phones. The antenna configuration is described in Section 2. The parameter studies and experiment results are described in Section 3. The conclusion is presented in Section 4.

2. ANTENNA CONFIGURATION

The proposed printed dual-band antenna is printed on an FR4 substrate that has dielectric constant 4.2, losstangent 0.02, and thickness 0.8 mm (see Fig. 1). The antenna consists of a bent inverted F antenna for the GSM band and a stub for the DCS band. The bent inverted F antenna is printed on the front of the substrate. The stub is etched on the back of the substrate, and the left end of the stub is connected to the left of the bent antenna through a via-hole. The upper section of the bent inverted F antenna is patterned on a side of the substrate. The end section of the antenna overlaps with the right part of the stub. This overlapped region induces a capacitor loading effect. Total antenna length and the capacitor loading effect generate a resonant mode at lower frequency; the length of the stub and the capacitor loading effect form a resonance mode at higher frequency. To generate a resonance at about 900 MHz for GSM operation, the total length of the antenna should be a quarter wavelength of the resonance frequency (about 83 mm). The feeding point is located at a distance (f) from the left end of the antenna. The feeding position influences impedance matching and the resonance frequencies, as occurs in a general inverted F antenna. The line width of the antenna is 0.5 mm and the total antenna size without ground plane has width $a = 35$ mm

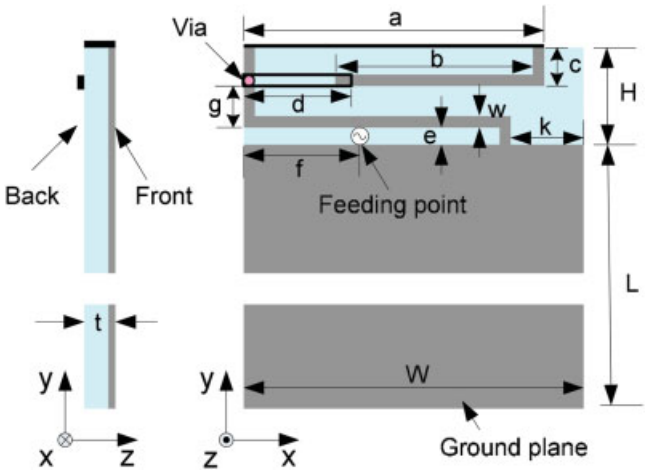

Figure 1 Configuration of the proposed printed dual-band antenna. [Color figure can be viewed in the online issue, which is available at www.interscience.wiley.com]