$(1/3) \times$ VDD-to-$(3/2) \times$ VDD Wide-Range I/O Buffer Using 0.35-μm 3.3-V CMOS Technology

Chi-Chun Huang, *Student Member, IEEE*, Tzung-Je Lee, Wei-Chih Chang, and Chua-Chin Wang, *Senior Member, IEEE*

***Abstract*—A 0.9/1.2/1.8/2.5/3.3/5.0-V wide-range input/output buffer carried out using a typical complementary metal–oxide–semiconductor (MOS) 2P4M 0.35-μm process is proposed in this brief. An input buffer with a logic calibration circuit is used for receiving a low voltage signal. A novel floating n-well circuit is employed to remove the body effect at the output p-channel MOS (PMOS). Moreover, a dynamic driving detector is included to equalize the turn-on voltages for the output PMOS and n-channel MOS transistors. The worst-case duty cycle of the output signal can then be 54.2% in a low-voltage mode. The maximum output frequency of the proposed design is measured to be 17.9/27.9/35.3/70.1/79.2/60.0 MHz for VDDIO $= 0.9/1.2/1.8/2.5/3.3/5.0$ V, respectively. The power consumption is 553 nW at the worst simulation case of [SS, 100 °C] and 330 nW by on-silicon measurement.**

***Index Terms*—Floating n-well, gate tracking, input/output (I/O) buffer, level converter, mixed-voltage tolerant.**

I. Introduction

RAPID development of semiconductor technologies causes the dimensions and supply voltages of transistors to be quickly scaled down to reduce the area cost and power consumption. During such an evolution, many chips on a printed-circuit-board-based system are fabricated by different technologies. Moreover, voltage difference might exist among different buses in one system. A signal voltage-level compatibility problem appears when those chips are used to communicate with one another since the voltage levels of these chips might be different. Traditional I/O buffers are no longer adequate to these different voltage-level signals due to the hazards of gate-oxide overstress, hot-carrier degradation, and unwanted leakage current paths [1]–[4]. By contrast, mixed-voltage I/O buffers are considered as a better solution to reduce the time-to-market than extra off-chip level shifters. Three types of mixed-voltage I/O buffers have been reported in prior works.

Type-I mixed-voltage I/O buffer is able to receive the signals at $2 \times$ VDD, [3]–[7]. By using stacked n-channel MOS (NMOS) transistors, the gate-oxide overstress at the output NMOS transistor can be avoided when $2 \times$ VDD is received. The aforementioned stacked NMOS and leakage elimination methodologies are only activated when $2 \times$ VDD appears in the receiving mode. Thus, a Type-I mixed-voltage I/O buffer can receive the high voltage signal, but it cannot transmit a high voltage signal, let alone a $2 \times$ VDD signal.

Type-II mixed-voltage I/O buffers, which can transmit high voltage signals, were disclosed in [8]–[10]. To avoid the gate-oxide overstress, two individual stacked p-channel MOS (PMOS) and NMOS are used in the output stage. However, these designs ignore the problem of the unwanted leakage current paths when a high voltage signal is biased at the PAD in the receiving mode.

Type-III mixed-voltage I/O buffer can transmit and receive signals with high, normal, and low voltage levels (VDDH, VDD, and VDDL) by including the aforementioned methodologies [11]–[14]. However, the I/O buffer can only communicate with the signal $\approx 1/2 \times$ VDD. When the supply voltage (VDDIO) is scaled down to be lower than 1/2 $\times$ VDD, the output signal is difficult to be pulled up to the required I/O voltage (VDDIO) due to the body effect of the output PMOS and the low turn-on voltages (Vgs) for the output NMOS.

This work proposes a very wide range I/O buffer using a 0.35-μm 3.3-V CMOS process, which can transmit and receive the signal of 0.9/1.2/1.8/2.5/3.3/5.0 V without any gate-oxide overstress and leakage current. The lower bound of the operating voltage is extended to be almost 0.27 $\times$ VDD. The output frequencies for VDDIO $= 0.9/1.2/1.8/2.5/3.3/5.0$ V are measured to be 17.9/27.9/35.3/70.1/79.2/60.0 MHz, respectively, at a given capacitive load of 30 pF.

II. Very Wide Range I/O Buffer

Fig. 1(a) shows the schematic of the proposed I/O buffer. The problems of possible gate-oxide overstress and unwanted leakage current can be avoided by employing the output stage composed of stacked transistors and dynamic gate bias generator, gate tracking, and floating n-well circuit.

For operation at VDDIO $\leq (1/2) \times$ VDD, there are two problems to be conquered. First, the output PMOS PM202 has a body effect by using the traditional floating n-well circuit, which biases the n-well at 3.3 V in the transmitting mode for all different VDDIOs. Second, when VDDIO is biased at VDDL$(= 0.9/1.2/1.8/2.5$ V), the turn-on voltage supplied for the output PMOS would be smaller than that for the output NMOS, which is controlled by a 3.3-V signal DN. These two problems reduce the driving current I_{OH} such that the duty cycle of the output signal will be deviated from 50% when

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The authors are with the Department of Electrical Engineering, National Sun Yat-Sen University, Kaohsiung 80424, Taiwan (e-mail: ccwang@ee.nsysu.edu.tw).

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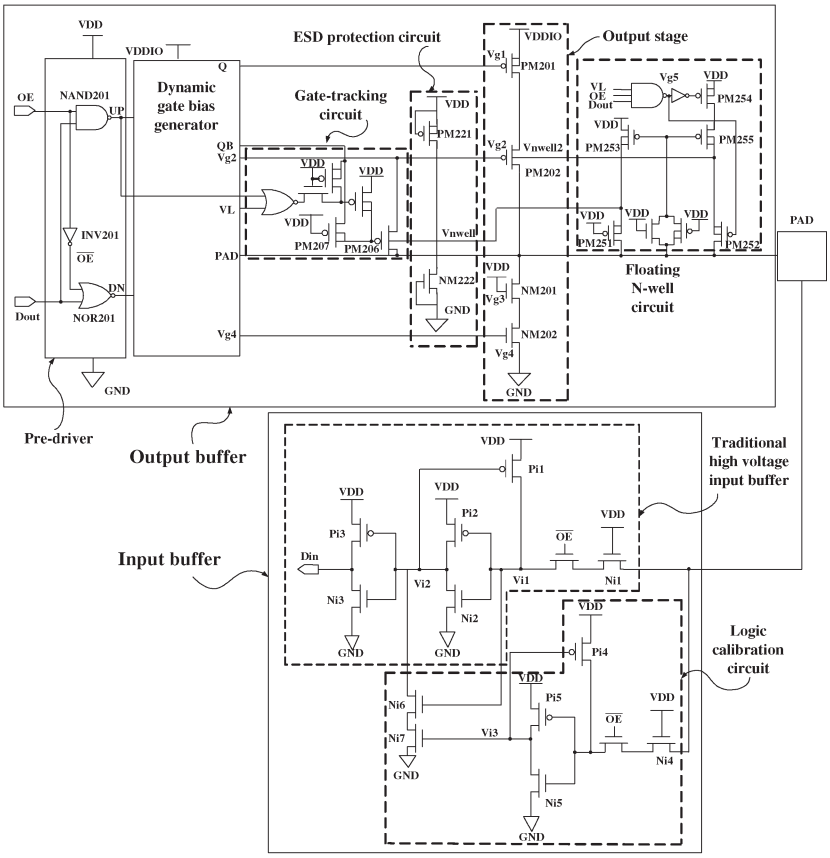

Operating mode	VDDIO	Vg1	Vg2	Vg3	Vg4
Receiving mode	0.9 V	0.9 V	3.3/5.0 V*	3.3 V	0 V
	1.2 V	1.2 V	3.3/5.0 V*	3.3 V	0 V
	1.8 V	1.8 V	3.3/5.0 V*	3.3 V	0 V
	2.5 V	2.5 V	3.3/5.0 V*	3.3 V	0 V
	3.3 V	3.3 V	3.3/5.0 V*	3.3 V	0 V
	5.0 V	5.0 V	3.3/5.0 V*	3.3 V	0 V
Transmitting mode (logic 1/0)	0.9 V	0/0.9 V	0/3.3 V	3.3 V	0/0.9 V
	1.2 V	0/1.2 V	0/3.3 V	3.3 V	0/1.2 V
	1.8 V	0/1.8 V	0/3.3 V	3.3 V	0/1.8 V
	2.5 V	0/2.5 V	0/3.3 V	3.3 V	0/2.5 V
	3.3 V	0/3.3 V	0/3.3 V	3.3 V	0/3.3 V
	5.0 V	>1.7/5.0 V	>1.7/3.3 V	3.3 V	0/3.3 V

*When V_{PAD} = 5 V, Vg2 must be biased at 5 V in the receiving mode.

(b)

VDDIO	UP	VL	Q	QB
5.0 V	0 V	0 V	2.5 V	5.0 V
	3.3 V		5.0 V	2.5 V
3.3 V	0 V	3.3 V	0 V	3.3 V
	3.3 V		3.3 V	0 V
2.5 V	0 V	3.3 V	0 V	2.5 V
	3.3 V		2.5 V	0 V
1.8 V	0 V	3.3 V	0 V	1.8 V
	3.3 V		1.8 V	0 V
1.2 V	0 V	3.3 V	0 V	1.2 V
	3.3 V		1.2 V	0 V
0.9 V	0 V	3.3 V	0 V	0.9 V
	3.3 V		0.9 V	0 V

(c)

VL	OE	Dout	DN	Vg5	Vnwell	Vnwell2
0 V	0 V	0 V	0 V	3.3 V	5.0 V	5.0 V
0 V	0 V	3.3 V	0 V	3.3 V	5.0 V	5.0 V
0 V	3.3 V	0 V	3.3 V	3.3 V	5.0 V	5.0 V
0 V	3.3 V	3.3 V	0 V	3.3 V	5.0 V	5.0 V
3.3 V	0 V	0 V	0 V	3.3 V	3.3 V	3.3 V
3.3 V	0 V	3.3 V	0 V	3.3 V	3.3 V	3.3 V
3.3 V	3.3 V	0 V	3.3 V	3.3 V	3.3 V	3.3 V
3.3 V	3.3 V	3.3 V	0 V	0 V	3.3 V	Tracing V_{PAD}

(d)

Fig. 1. Proposed mixed-voltage-tolerant I/O buffer. (a) Schematic of the proposed I/O buffer. (b) Truth table for gate voltages of the output stage. (c) Truth table for the outputs of the voltage-level converter. (d) Truth table for the outputs of the floating n-well circuit.

VDD = VDDL. It might cause missing codes, which should be avoided in all kinds of digital systems.

A. Theory of the Proposed I/O Buffer

The proposed design employs a new floating n-well circuit, which provides a dynamic n-well voltage (Vnwell2), to avoid the body effect by tracing PM202's source voltage in the transmitting mode for VDDIO = VDDL. Moreover, a dynamic driving detector, as shown in Fig. 2, is used to generate Vg4 with an amplitude of VDDIO for the output NMOS when VDDIO = VDDL. Thus, the turn-on voltages could be equalized. Moreover, the function of gate tracking should be turned off in the transmitting mode for VDDIO = 5.0 V. Otherwise, the driving current of PM202 would gradually be reduced when the output signal $V_{\rm PAD}$ rises toward 5.0 V. Thus, the output duty cycle will be very close to 50% for all VDDIOs.

On the other hand, because 1.8 V is very close to the switch point of 3.3-V logic circuits, an input buffer with a logic calibration is used to receive the signal with an amplitude less than 1.8 V.

Moreover, a dc bias required in the dynamic gate bias generator is very important for low-power operation. Many prior works use a simple MOS resistor string, which results in a tradeoff between the stability and the power consumption caused by the dc operation current. Using diode-connected MOS and charge redistribution topology might cause a penalty of circuit complexity. In this brief, a low-power clamping bias circuit with a low operation current is used to provide a stable dc voltage [11].

B. Schematic Design of the Proposed I/O Buffer

The details of each subcircuit in the proposed I/O buffer are disclosed as follows.

Predriver: The predriver is in charge of predriving and decoding. When OE = 3.3 V, the output signal $Dout$ would be transmitted. In this case, UP and DN will be both biased at 3.3 V (0 V) for $Dout$ = 0 V (3.3 V). When OE = 0 V, the I/O buffer is in the receiving mode, and UP and DN would be biased at 3.3 and 0 V, respectively.

Output Stage: The output stage is composed of the stacked PMOS, i.e., PM201 and PM202, and the stacked NMOS, i.e., NM201 and NM202. In addition to the stacked transistor strings, the output stage requires appropriate gate bias voltages to avoid gate-oxide overstress and correctly operate for different VDDIOs, as shown in the truth table in Fig. 1(b). In the receiving mode, Vg1 is biased at VDDIO to turn PM201 off. In the mean time, Vg2, Vg3, and Vg4 are biased at 3.3, 3.3, and 0 V, respectively. Notably, when $V_{\rm PAD}$ = 5.0 V, Vg2 should be pulled to 5.0 V by the gate-tracking circuit to avoid the leakage current path through PM202. In the transmitting mode, Vg1 and Vg2 are biased at the voltage larger than 1.7 V (= 5.0 − 3.3 V) for VDDIO = 5.0 V and biased at 0 V for other VDDIOs. Thus, logic 1 can be transmitted, and the gate-oxide overstress is avoided. For transmitting logic 0, Vg4 is biased at VDDIO when VDDIO = VDDL or VDD to equalize turn-on gate-source voltages for the output transistors PM201 and NM202. These gate

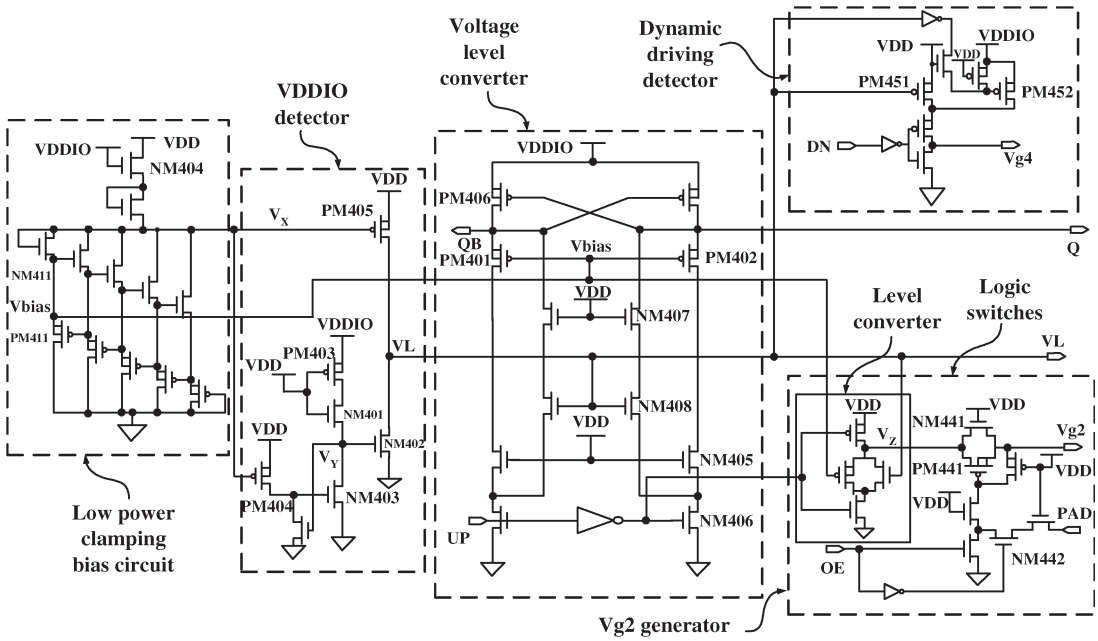

Fig. 2. Proposed dynamic gate bias generator.

bias voltages are provided by the dynamic gate bias generator.

Dynamic Gate Bias Generator: The dynamic gate bias generator is composed of a low-power clamping bias circuit, a VDDIO detector, a voltage-level converter, a Vg2 generator, and a dynamic driving detector, as shown in Fig. 2.

Low-Power Clamping Bias Circuit: The low-power clamping bias circuit provides a 1.7-V output (Vbias) for the voltage-level converter and Vg2 generator. The low-power clamping bias circuit is composed of five stages of serial NMOS and PMOS. The common source node of the PMOS and NMOS in each stage is clamped at a steady voltage. If the voltage of the common source node is initially higher than the expected threshold, it would be discharged by the PMOS. Contrarily, if the voltage of the node is initially low, it would be charged by the corresponding NMOS. Hence, the voltage of the common source node in each stage is clamped at a predefined value. Therefore, Vbias can be tuned to be 1.7 V, which is about five times the threshold voltage of the PMOS.

VDDIO Detector: The VDDIO detector can provide an output signal VL, which is 0 V for VDDIO $= 5.0$ V and 3.3 V for other VDDIOs. Thus, it can determine the VDDIO mode and ensure the functional correctness of the I/O buffer. When VDDIO $= 5.0$ V, PM403 and PM401 are turned on. V_Y is then pulled high to turn on NM402. Additionally, NM404 is turned on to pull V_X high such that PM405 is off. Therefore, VL is discharged to 0 V. When VDDIO $=$ VDDL or VDD, PM404 and NM403 would be turned on such that V_Y would be discharged to 0 V. It turns off NM402. Moreover, PM405 is turned on, because V_X is pulled low. Therefore, VL is biased at 3.3 V for VDDIO $=$ VDDL or VDD.

Voltage-Level Converter: The voltage-level converter receives the control signal UP with a voltage level of 3.3 V and generates a pair of complementary signals Q and QB, as shown in the truth table in Fig. 1(c). When VDDIO $= 5.0$ V and UP $=$ 0 V, NM405 and NM406 are turned on, and Q is discharged through PM402, NM405, and NM406. Because Vbias is 1.7 V, Q would be clamped at 2.5 V $(= 1.7\text{ V} + |V_{\text{th,PM402}}|)$. It turns on PM406 and pulls QB to 5.0 V so as to avoid the gate-oxide overstress at PM406. By contrast, Q and QB are biased at 5.0 V and 2.5 V for UP $= 3.3$ V, respectively. When VDDIO $=$ $0.9-3.3$ V and UP $= 0$ V, Q is discharged to 0 V through NM407, NM408, and NM406 such that QB is pulled to VDDIO $(= 0.9-3.3\text{ V})$ by PM406. Similarly, when UP $= 3.3$ V, Q and QB are biased at 0.9–3.3 and 0 V, respectively.

Vg2 Generator: The Vg2 generator is composed of a level converter and logic switches. The level converter is similar to the voltage-level converter, which receives the control signal UP, and generates a level-shifted signal V_Z at 2.5 V when VDDIO $= 5.0$ V and UP $= 0$ V. For VDDIO $=$ VDDL or VDD, V_Z is equal to UP. The logic switches bias Vg2 at V_Z or at V_{PAD} according to the control signal OE and V_{PAD}. When OE $= 0$ V (receiving mode) and $V_{\text{PAD}} = 5.0$ V, PM441 is turned off. Vg2 is determined by the gate-tracking circuit, and NM441 and PM441 would protect the internal transistors from the high voltage of 5.0 V. For all other cases, Vg2 is coupled to V_Z and separated from V_{PAD} by turning off NM442.

Dynamic Driving Detector: When VDDIO $= 5.0$ V, VL is biased at 0 V such that PM451 is on and PM452 is off. Then, Vg4 is biased at 3.3 V through PM451. When VDDIO $=$ VDDL and VDD, VL is at 3.3 V such that PM451 is off and PM452 is on. Thus, Vg4 is pulled to VDDIO through PM452. Therefore, Vg4 can be biased at the voltage shown in Fig. 1(b).

Gate-tracking Circuit: The schematic of the gate-tracking circuit is shown in Fig. 1(a). In the receiving mode, the gate-tracking circuit monitors V_{PAD}. When $V_{\text{PAD}} = 5.0$ V, PM206 would be turned on, and Vg2 can be pulled up to 5.0 V through PM206 such that the leakage current path through PM202 is blocked. In the transmitting mode, PM207 would be turned on for VDDIO $= 5.0$ V. Then, the gate of PM206 will be biased at 5.0 V such that V_{PAD} cannot be coupled to Vg2.

Floating n-well Circuit: Referring to Fig. 1(a), the floating n-well circuit receives the control signals VL, OE, Dout,

and $V_{\rm PAD}$. Vnwell is similar to the traditional floating n-well voltage to trace $V_{\rm PAD}$ in the receiving mode. Notably, Vnwell2 can trace $V_{\rm PAD}$ when transmitting logic 1, which is totally different from any prior work. Hence, the body effect on PM202 can be removed, and the driving current is enhanced. When VDDIO is at VDDL or VDD and logic 1 is transmitted, the gate of PM252 is biased at 0 V such that Vnwell2 is equal to $V_{\rm PAD}$. Therefore, the n-well voltage of PM202 can trace its drain and source voltage such that the body effect is eliminated. At the same time, Vnwell is biased at 3.3 V by PM253. When 5.0 V is transmitted, the gate of PM252 is biased at 3.3 V. PM251 and PM252 would be turned on such that Vnwell and Vnwell2 are both biased at 5.0 V by $V_{\rm PAD}$. The leakage current paths through the parasitic diodes of PM202 and PM206 are then closed. Similarly, Vnwell and Vnwell2 can be biased at 5.0 V for $V_{\rm PAD} = 5.0$ V in the receiving mode through PM251 and PM252, respectively. For all other cases in the receiving mode, Vnwell and Vnwell2 are biased at 3.3 V through PM253 and PM254, as well as PM255, respectively.

Input Buffer: The input buffer is composed of a traditional high-voltage input buffer, which can receive the input signal with a high voltage without any gate oxide overstress, and a logic calibration circuit. By properly tuning the aspects of the transistors, the traditional high-voltage input buffer can receive 1.8-V signal. However, when $V_{\rm PAD} = 0.9$ V or 1.2 V, Vi2 would be biased at 3.3 V, and Din is at 0 V to cause a logic error since the switching voltage of the inverter, Pi2 and Ni2, is higher than 1.2 V. The logic error is resolved by adding the logic calibration circuit. When $V_{\rm PAD} = 1.2$ V or 0.9 V, Vi3 is biased at 3.3 V to turn on Ni7 such that Vi2 can be pulled to 0 V by Ni7 and the feedback loop composed of Pi1, Pi2, and Ni2. Then, the logic error can be corrected.

ESD Protection Circuit: Although the output stage is composed of the stacked transistors, the HBM ESD level from VDDIO to PAD is still larger than most of the commercial requirements, i.e., 2 KV, by attaining the aspect ratio of 880 μm/0.35 μm and 216 μm/0.35 μm for the output PMOS and NMOS transistors, respectively. However, the ESD strength from PAD to VDD will be weak if no ESD circuit is used. Thus, a pair of gate-source-coupled transistors NM222 and PM221 is employed to improve the HBM ESD level for PAD-to-GND and PAD-to-VDD modes. Notably, the node between NM222 and PM221 need not be connected to any other node, as shown in Fig. 1(a). By tuning the aspect ratio, the ESD protection circuit will bypass the current via GND and VDD.

III. Implementation and Measurement

The proposed design is implemented using a typical 0.35-μm 2P4M CMOS process. Fig. 3 shows the die photo and layout of the proposed I/O buffer, where IO1 is the proposed buffer, IO2 is the same as IO1 with several observable outputs, and IO3 does not include any ESD protection circuit for the testing purpose. The area of the proposed circuit is 0.497×0.111 mm^2.

Fig. 4 shows the measured waveforms of $V_{\rm PAD}$, Vnwell, Vg2, and Vnwell2 in the receiving mode. When the receiving signal $V_{\rm PAD}$ is biased at 5.0 V, Vnwell, Vnwell2, and Vg4 are pulled to 5.0 V by a floating n-well circuit and a gate-tracking

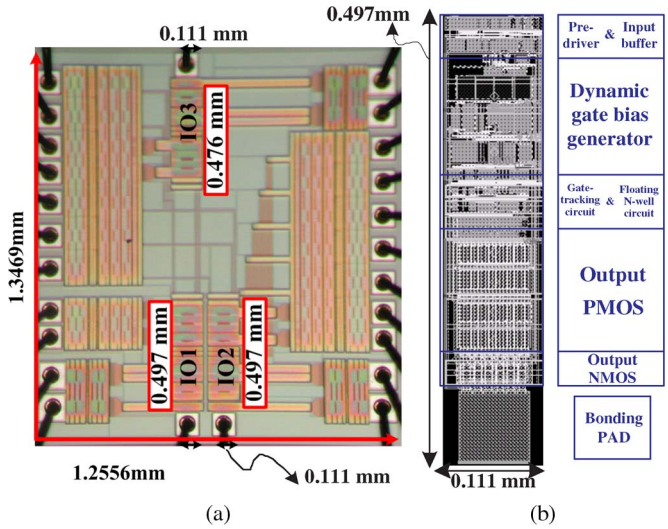

Fig. 3. Die photo and layout of the proposed design. (a) Die photo. (b) Layout.

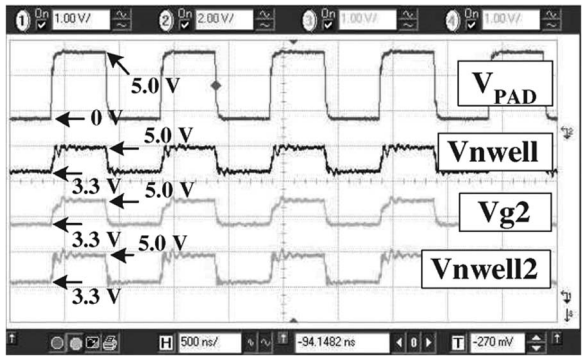

Fig. 4. Measured waveforms of $V_{\rm PAD}$, Vnwell, Vg2, and Vnwell2 in the receiving mode for a 5.0-V 1-MHz signal is given at $V_{\rm PAD}$.

circuit, respectively. Thus, the unwanted leakage current paths are blocked.

Fig. 5 shows the measured full-swing waveforms of the output signal $V_{\rm PAD}$ at the maximum operating frequency. The maximum operating frequency for VDDIO $= 0.9/1.2/1.8/2.5/3.3/5.0$ V are 17.9/27.9/35.5/70.1/79.2/60.0 MHz, respectively, given a 30-pF load. Moreover, the duty cycle are measured to be 54.2% for the worst case when VDDIO $= 5.0$ V. The static power consumption is 553 nW at the worst simulation corner of the SS model and 100 °C for VDDIO $= 5.0$ V [15]. Since the resolution of the measurement equipment Picotest M3500A is 100 nA and VDD $= 3.3$ V, we can conclude that the max power is less than 330 nW.

Table I reveals the specification comparison of the proposed design with prior works. Because only two stacked PMOS and NMOS transistors are used in the output stage, the area is much smaller than that of [10]. In addition, the proposed design is the only one that can be applied to six different voltage modes without using any thick-oxide devices.

IV. Conclusion

A 0.9/1.2/1.8/2.5/3.3/5.0-V very wide range I/O buffer has been proposed in this brief. The proposed I/O buffer can provide six VDDIO modes for transmitting and receiving without any gate-oxide overstress and leakage current path. By eliminating the body effect of the output PMOS and equalizing the turn-on

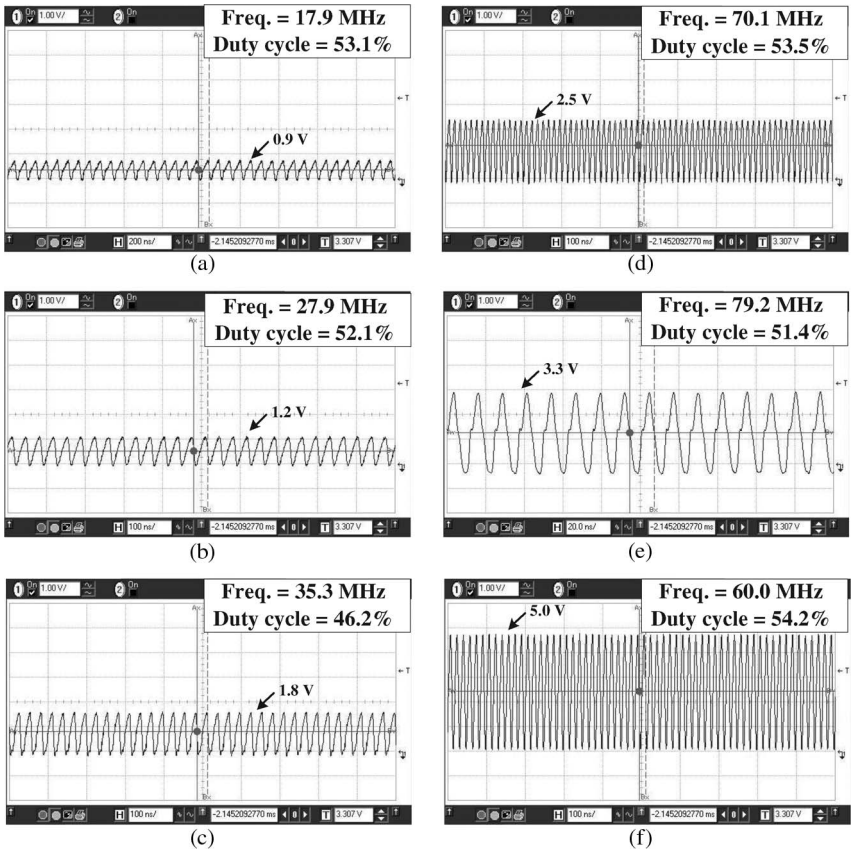

Fig. 5. Measured waveforms of the output signal V_{PAD} at the maximum frequency for different VDDIOs. (a) VDDIO $= 0.9$ V. (b) VDDIO $= 1.2$ V. (c) VDDIO $= 1.8$ V. (d) VDDIO $= 2.5$ V. (e) VDDIO $= 3.3$ V. (f) VDDIO $= 5.0$ V.

TABLE I
COMPARISON WITH SEVERAL PRIOR WORKS

	[5]	[6]	[8]	[10]	[11]	This work
# of voltage modes	2	2	1	1	3	6
Tx VDDH	No	No	Yes	Yes	Yes	Yes
Tx VDDL	No	No	No	No	Yes	Yes
Rx VDDH	Yes	Yes	No	No	Yes	Yes
Rx VDDL	No	No	No	No	Yes	Yes
Max. operating voltage	2·VDD	3·VDD	3.3·VDD	3·VDD	1.5·VDD	1.5·VDD
Min. operating voltage	VDD	VDD	3.3·VDD	3·VDD	0.54·VDD	0.27·VDD
Output stage	1P2N	1P1N	2P2N	3P3N	2P2N	2P2N
Thick-oxide	No	No	Yes	No	No	No
Normal Voltage (VDD)	2.5 V	1.0 V	1.0 V	2.5 V	3.3 V	3.3 V
Process	0.25 um	0.13 um	0.13 um	0.25 um	0.35 um	0.35 um
Area (mm^2)	N/A	0.0105	0.0316	5.76	0.0336	0.0497
Year	2006	2006	2007	2005	2009	2009

voltage for output PMOS and NMOS, the proposed I/O buffer can generate output the signal with 54.2% duty cycle in the worst case. In addition, the power consumption of the proposed design is only 553 nW by using the low-power clamping bias circuit.

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