

A linear LDO regulator with modified NMCF frequency compensation independent of off-chip capacitor and ESR

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Abstract This paper presents a novel compensation design for regulators, i.e., modified NMCF (nested Miller compensation with feedforward Gm stage), resulting in a linear LDO (low dropout) regulator whose performance is independent of the off-chip capacitor and its ESR (equivalent series resistor). The proposed compensation method ensures the stability of the feedback loop and the sufficient phase margin of the LDO regulator. Besides, the transient response become faster. The analysis of the stability is derived to solidify the proposed design. The proposed design is implemented using TSMC 0.35 μm 2P4M CMOS process. The results verify the performance and the stability on silicon. The power supply rejection ratio is 25 dB @ [200 Hz, 3 MHz], [50 Ω , 500 Ω] provided that the input voltage varies from 4 to 5 V.

Keywords LDO regulator · Modified NMCF · Frequency compensation · ESR

1 Introduction

The LDO (low-dropout) regulator is generally utilized to translate a voltage level or provide a stable output voltage, which has been considered as one of the important

components for the power management of wireless applications, e.g., cellular phones, hand-held computers, battery charging [1, 2] and particularly implanted wireless biomedical chips [3]. Traditional linear LDO regulators usually consist of a two-stage error amplifier, a power output stage and a negative feedback loop. However, since the stability and accuracy of the regulated output voltage is the most critical factor in many field applications such as biomedical chips, traditional designs suffer from poor efficiency as the difference between the input and output voltages is increased [4]. In order to attain a fast transient response and an accurate output voltage, several prior LDO regulators were proposed to use high gain amplifiers with a cascade or cascode technology. It results in the stability problem due to the appearance of inherent three poles. Besides, the varying load current also affects the stability [5, 6]. Thus, a frequency compensation technique to ensure the stability of the LDO regulator was proposed to resolve this problem [5–7]. Otherwise, the circuitry will become unstable due to the inherent three poles if there is no any compensation mechanism. What worse is that the equivalent loading impedance of the LDO regulator might not be a constant. It then leads to the output pole drifting. Thus, the loop stability of the LDO regulator is uncertain. An off-chip capacitor C_{off} , as shown in Fig. 1, was proposed to maintain the stability of the LDO regulator in several research works, [4, 8, 9]. The off-chip capacitor and its ESR (equivalent series resistor) are designed to move the zero to achieve a pole-zero cancellation and keep the phase margin larger than zero degree [10]. However, the off-chip capacitor increases the area of printed-circuit board and the value of the ESR might drift owing to the variation of the temperature and different materials [11]. Therefore, the off-chip capacitor scheme is also not deemed as a reliable solution. In this work, a new compensation method independent of the off-chip capacitor and its ESR is

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presented to enhance the LDO regulator’s performance regarding the transient response and the noise rejection.

2 LDO regulator using NMCF

A traditional LDO regulator is shown in Fig. 1, where a bandgap bias circuit generates a PVT(process, supply voltage, temperature)-independent reference voltage V_{ref} . The series resistors, R_{cf1} , R_{cf2} , monitor the output voltage by a simple voltage division. A feedback voltage V_{fb} is fed back to be compared with V_{ref} by the error amplifier. The error amplifier then feeds a control voltage into the pass transistor M_{cpass} to regulate the output voltage according to the difference between V_{ref} and V_{fb} . The faster speed of the feedback loop comes along with the more stable output voltage. Therefore, a large gain is required to ensure that the feedback loop stays stable. Hence, the frequency compensation becomes a critical issue in the LDO regulator design. However, there is a trade-off between the loop gain and the bandwidth of the circuit.

2.1 Modified NMCF compensation

The structure of the proposed LDO regulator is shown in Fig. 2. It is composed of two cascaded error amplifiers, A_{op1} , A_{op2} , a pass transistor, M_{pass} , series resistors, R_{f1} , R_{f2} , two compensation capacitors, C_{m1} , C_{m2} , and a feedforward transconductance amplifier stage, A_{opf} . What we propose is to insert a feed forward Gm boosting amplifier between the output of the first error amplifier and the resistor-based voltage divider. Meanwhile, two compensation capacitors are added on the source and the drain of the pass element to mimic the Miller capacitor compensation. It is then called the modified NMCF (nested Miller compensation with feedforward Gm stage) design.

In order to simplify the analysis of the frequency compensation, we assume that g_{mi} , R_{oi} are the transconductance

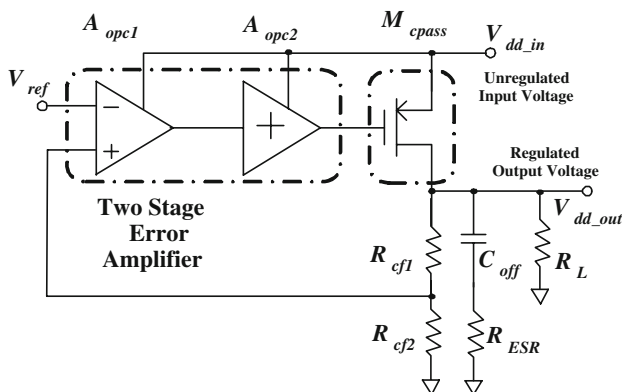


Fig. 1 The classical LDO regulator with the off-chip capacitor

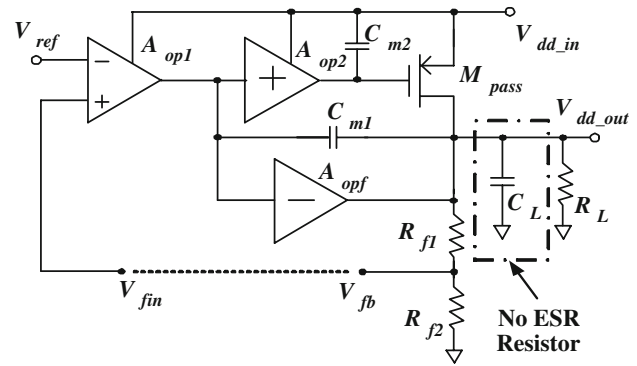


Fig. 2 The structure of the proposed LDO regulator

and the output impedance of the amplifier A_{opi} , respectively, where $i = 1, 2$, or f . g_{mp} and R_{op} denote the transconductance and the output impedance of the transistor M_{pass} , respectively. Besides, we assume that the gain of each amplifier is much larger than the unit gain. The load capacitor, C_L , and the compensation capacitors are much larger than parasitic capacitors which could be neglected in the analysis.

Based on these assumptions, the open loop transfer function is given by

$$T(s) = \frac{V_{fb}(s)}{V_{fin}(s)} = \frac{TDC \cdot \text{Zero}(s)}{\left(1 + \frac{s}{p_1}\right)\left(1 + \frac{s}{p_2}\right)\left(1 + \frac{s}{p_3}\right)},$$

$$TDC = (g_{m1}g_{m2}g_{mp}R_{o1}R_{o2})\left(\frac{R_{op}R_L}{R_{op} + R_L}\right)\left(\frac{R_{f2}}{R_{f1} + R_{f2}}\right),$$

$$p_1 = \frac{R_{op} + R_L}{C_{m1}g_{m2}g_{mp}R_{o1}R_{o2}R_{op}R_L},$$

$$p_2 = \frac{1}{R_{o2}C_{m2}},$$

$$p_3 = \frac{R_{op} + R_L}{R_{op}R_L C_L},$$

$$\text{Zero}(s) = 1 + \left(\frac{g_{mf}C_{m2}}{g_{m2}g_{mp}}\right)s - \left(\frac{C_{m1}C_{m2}}{g_{m2}g_{mp}}\right)s^2, \tag{1}$$

where TDC is the DC loop gain, and p_1 is the dominant pole.

According to Eq. 1, the LHP zero is found to be as follows,

$$z_1 = -\frac{g_{mf}}{2C_{m1}}\left(\sqrt{1 + 4\frac{C_{m1}g_{m2}g_{mp}}{C_{m2}g_{mf}}} + 1\right). \tag{2}$$

By contrast, the RHP zero is also derived to be

$$z_2 = \frac{g_{mf}}{2C_{m1}}\left(\sqrt{1 + 4\frac{C_{m1}g_{m2}g_{mp}}{C_{m2}g_{mf}}} - 1\right). \tag{3}$$

The LHP zero should be located after p_2, p_3 for the stability purpose [7]. Thus, the following conditions must be held, given $C_{m1} \ll C_{m2}$, and $R_{op} \ll R_L$: $g_{mf} \geq \frac{C_{m1}}{R_{op}C_L}$, $g_{mf} \geq \frac{C_{m1}}{R_{o2}C_{m2}}$.

By setting p_2 and p_3 larger than the required GBW (gain-bandwidth product), the GBW is then found to be

Fig. 3 The schematic of the proposed LDO regulator

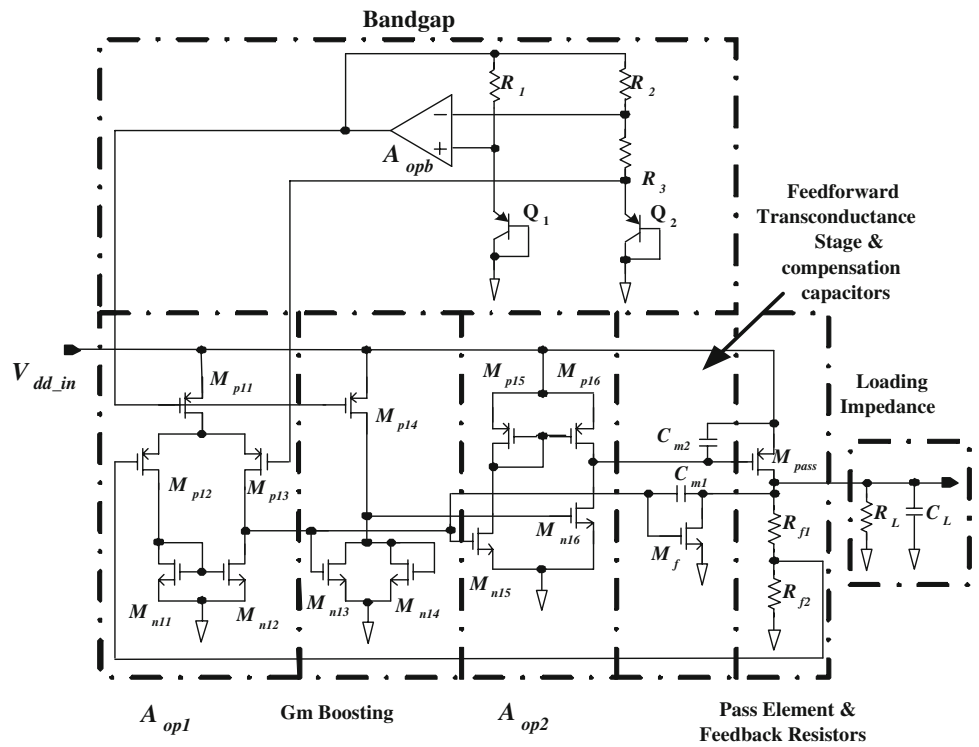
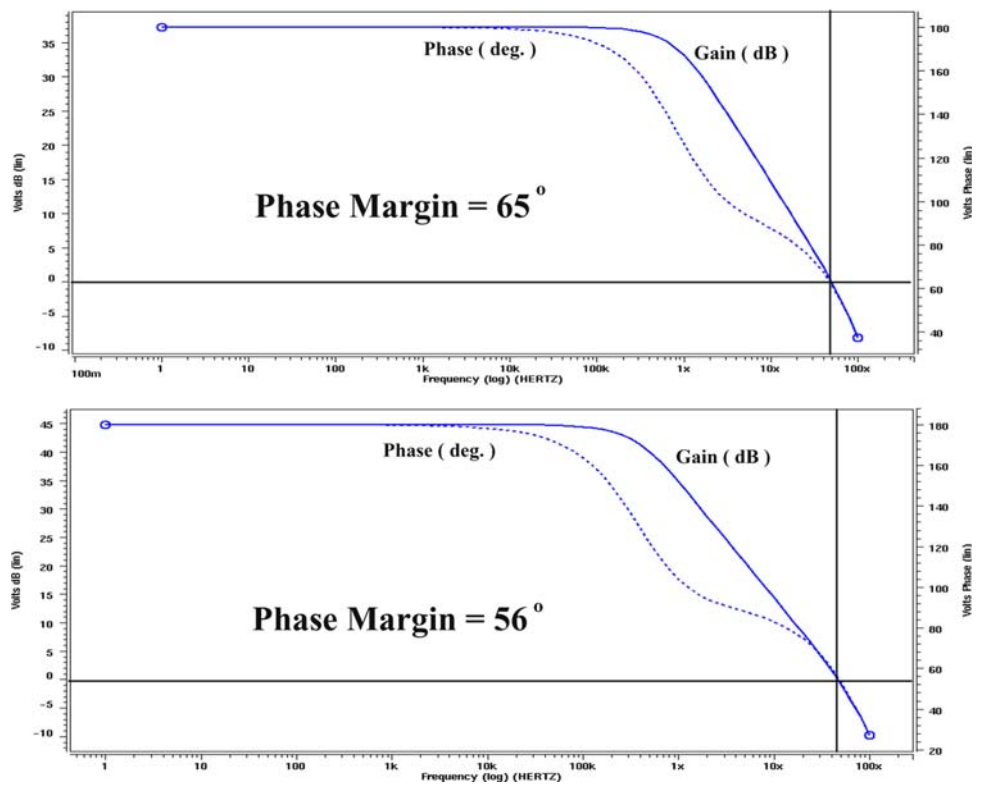


Fig. 4 Loop gain and loop phase at 0 and 75°C



$$GBW = \frac{g_{m1}}{C_{m1}} \tag{4}$$

The phase margin (*PM*) is also derived to be

$$PM \approx 90^\circ - \tan^{-1}\left(\frac{GBW}{p_2}\right) - \tan^{-1}\left(\frac{GBW}{p_3}\right) - \tan^{-1}\left(\frac{GBW}{z_2}\right) + \tan^{-1}\left(\frac{GBW}{|z_1|}\right) > 60^\circ \tag{5}$$

If the phase margin of a loop greater than 60°, the time domain response of this loop will get rid of ringing [12]. In short, a stable LDO regulator independent of the ESR can be attained by tuning *g_{mf}*, *C_{m1}* and *C_{m2}* despite that the load capacitor *C_L* varies.

2.2 Circuit design

The schematic of the proposed design is shown in Fig. 3. *R₁*, *R₂*, *R₃*, *Q₁*, *Q₂*, and *A_{opb}* act as the bandgap bias circuitry. The reference voltage is easily derived as

$$V_{ref} = V_{EB2} + \left(1 + \frac{R_2}{R_3}\right) V_t \ln\left(\frac{A_{Q2}}{A_{Q1}}\right) \tag{6}$$

where *A_{Q1}* and *A_{Q2}* are the emitter area of *Q₁* and *Q₂*, respectively. *M_{p11}* – *M_{p13}*, *M_{n11}*, and *M_{n12}* constitute the first stage of the error amplifier, *A_{op1}*, while *M_{p15}*, *M_{p16}*, *M_{n15}*, and *M_{n16}* construct the second stage, *A_{op2}*. *R_{f1}* and *R_{f2}* are the feedback series resistors. *C_{m1}* and *C_{m2}* are the compensation capacitors. *M_f* is the feedforward transconductance stage, i.e., *A_{opf}*, which generates a negative small signal to cancel the feedforward current passing through *C_{m1}* at high frequency. *M_{p14}*, *M_{n13}*, and *M_{n14}* are in charge of gm-boosting for the loop.

The pass transistor plays a critical role in the design of the LDO regulator. There are five types of pass transistors made up with different transistors to be chosen : Darlington pairs, NPN, PNP, NMOS, and PMOS. The first three components are bipolar junction transistors which could provide a large output current, but produce larger power consumption. Additionally, the dropout voltage is another important factor when it comes to the selection of the pass transistor. Since NMOS needs its gate voltage higher than its source voltage to get into the saturation region, the dropout voltage is high if it is used as the pass transistor. Therefore, PMOS is selected in the proposed design.

3 Simulation and implementation

We select the value of *C_{m1}* and *C_{m2}* to be equal to 0.1 and 30 pF, respectively, basing on the analysis of Eqs. 1–5. Figure 4 shows that the proposed design is stable in the temperature range [0, 75°C]. The PSRR (power supply rejection ratio) results given different *C_L* and *R_L* are shown in Figs. 5 and 6, respectively. Figure 7 shows the overall

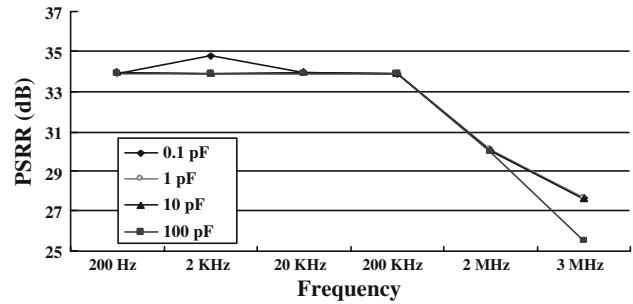


Fig. 5 PSRR of the proposed LDO regulator at different *C_L* (*R_L* = 100)

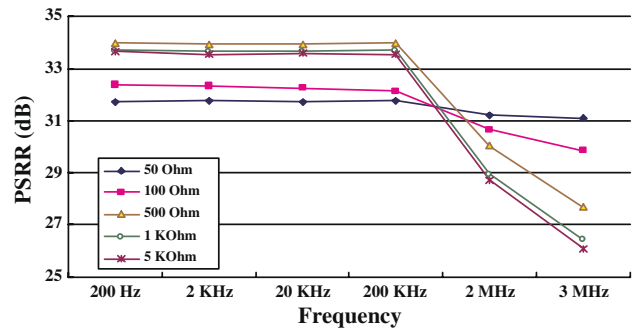


Fig. 6 PSRR of the proposed LDO regulator at different *R_L* (*C_L* = 10 pF)

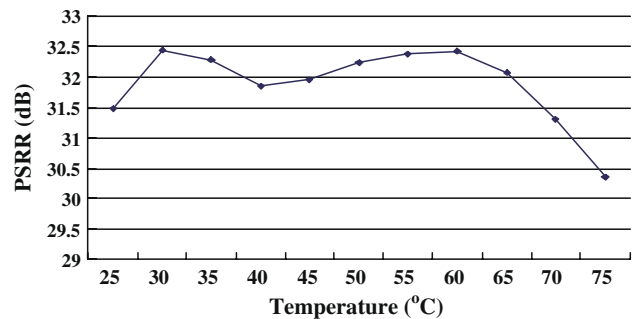


Fig. 7 PSRR of the proposed LDO regulator at [25, 75°C] (*R_L* = 100, *C_L* = 10 pF)

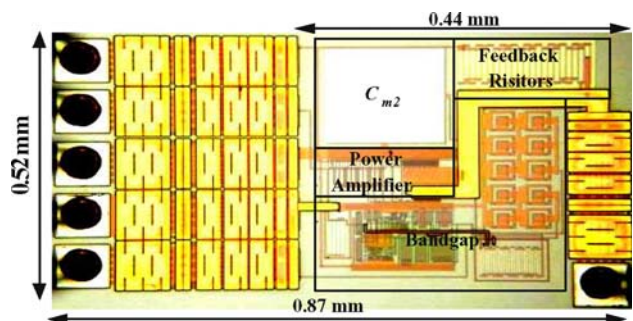


Fig. 8 Die photo of the proposed LDO Regulator

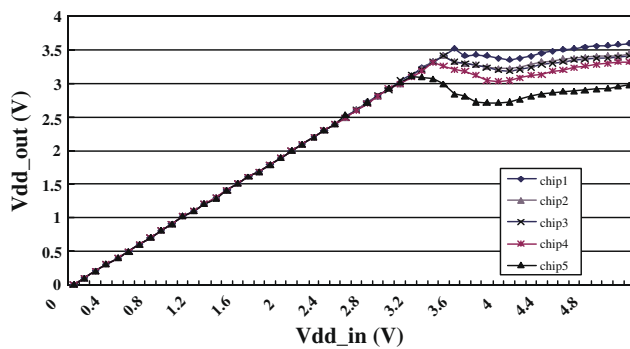


Fig. 9 Output voltage versus input voltage at different chips

Table 1 Performance comparison of LDO regulators

	[4]	[8]	Ours
PSRR (dB)	54	38	25
CMOS process (μm)	0.25	0.5	0.35
Chip area (mm^2)	0.21	1	0.45
Max. freq.	N/A	3 KHz	3 MHz
Max. O/P power (mW)	720	990	360
$V_{\text{dd_in}}$ ripple	N/A	N/A	1 V
Dropout voltage (V)	0.5	0.3	0.3
$C_{\text{off-chip}}$ needed	Yes	Yes	No
Applications	Battery-operated	DC-voltage-transferred	RF-power-transferred

PSRR given different temperatures. In short, the PSRR is 25 dB @ [200 Hz, 3 MHz], [50 Ω , } 500 Ω] provided that the input voltage varies from 4 to 5 V.

TSMC (Taiwan Semiconductor Manufacturing Company) 0.35 μm 2P4M CMOS process is adopted to carry out the proposed design. The die photo of the proposed LDO regulator is shown in Fig. 8 and the chip area is 870 $\mu\text{m} \times 520 \mu\text{m}$. Figure 9 shows the regulated output voltage $V_{\text{dd_out}}$ versus the input voltage $V_{\text{dd_in}}$ in different chips. Referring to Fig. 9, all $V_{\text{dd_out}}$ value of these chips varies from 3.0 to 3.6 V given $V_{\text{dd_in}}$ from 3.7 to 5.2 V except chip 5. It is good enough to be used in RF-power-transferred applications, e.g., RFID, wireless no battery implantable biomedical chips.

A performance comparison of the proposed design with several prior LDOs is summarized in Table 1. Our design provides the least dropout voltage, the maximum operation frequency without using any off-chip capacitor.

4 Conclusion

We have proposed a LDO regulator with a modified NMCF compensation design. Its outstanding performance is

independent of the off-chip capacitor and its ESR. The detailed compensation analysis of the proposed design is also revealed to illustrate the methodology. The simulation and measurement results justify that the supply ripple rejection is independent of the load resistor in the range from 50 Ω to 500 Ω . Moreover, the PSRR keeps 25 dB even if the operating frequency is up to 3 MHz.

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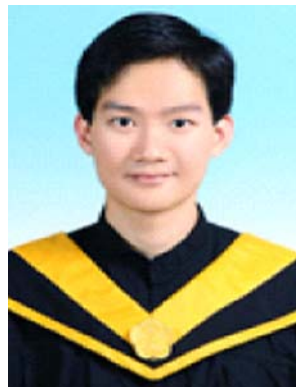
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