Transactions Briefs

A Wide Voltage Range Digital I/O Design Using Novel Floating N-Well Circuit

Chua-Chin Wang, Chia-Hao Hsu, Szu-Chia Liao, and Yi-Cheng Liu

***Abstract*—A fully bidirectional mixed-voltage input/output (I/O) buffer using a novel floating N-well circuit is presented. To provide appropriate gate voltages for output stage transistors, a dynamic gate bias generator without gate-oxide overstress effect is implemented. The proposed I/O also takes advantage of a novel gate-tracking circuit and a PAD voltage detector by means of eliminating the leakage current such that the compatibility among all subcircuits is ensured. Our design is proved on silicon using 0.18 μm CMOS process that when VDDIO is 5.0/3.3/1.8/1.2/0.9 V, the maximum data rate is found to be 80/80/125/100/80 MHz, respectively, with a given capacitive load of 10 pF.**

***Index Terms*—Dynamic gate bias, floating N-well, mixed-voltage, wide-range input/output (I/O) buffer.**

I. Introduction

Though the feature size of semiconductor processes and the core voltage are kept scaling down, the supply voltage on board is still remained as high as 3.3 V (or even 5.0 V), e.g., a PCI-X interface [1], [2]. Therefore, an input/output (I/O) cell capable of receiving/transmitting different signal voltages is very much needed. Prior I/O buffer schemes have been proved to be prone to potential problems of hot-carrier degradation, gate-oxide overstress, and undesirable leakage current paths in advanced processes and applications nowadays [3], [4]. For instance, I/O buffers proposed in [3]–[7] were meant to improve these effects where many efforts have been thrown thereon except that the best performance among these designs can be applied only to three different voltage modes.

Prior works, [2], [5]–[7], cannot support 1/2 to 3 times $V_{\rm DD}$ tolerance. Although [8] can achieve the same voltage tolerance capability, the speed is too slow. Therefore, the main goal of this work is focused on the speed enhancement. Comparing with the above papers, this work presents a high speed I/O buffer and widest voltage tolerant. The most attractive advantage in our design is a novel floating N-well circuit to facilitate a high data rate. In addition, our design given the supply voltage $V_{\rm DD} =$ 1.8 V is implemented by a standard CMOS 0.18-μm process using only thin-oxide devices for the fabrication cost reduction.

II. High-Speed Wide-Range Mixed-Voltage I/O Buffer

The proposed wide voltage range I/O buffer is shown in Fig. 1. The predriver is used to determine the proposed I/O buffer in either transmitting mode (Tx) or receiving mode (Rx). According to the biases of the High voltage detector and $V_{\rm PAD}$, a dynamic gate bias generator generates appropriate bias voltages for other subcircuits. A PAD voltage detector is used to ensure the gate-oxide reliability for the transistors

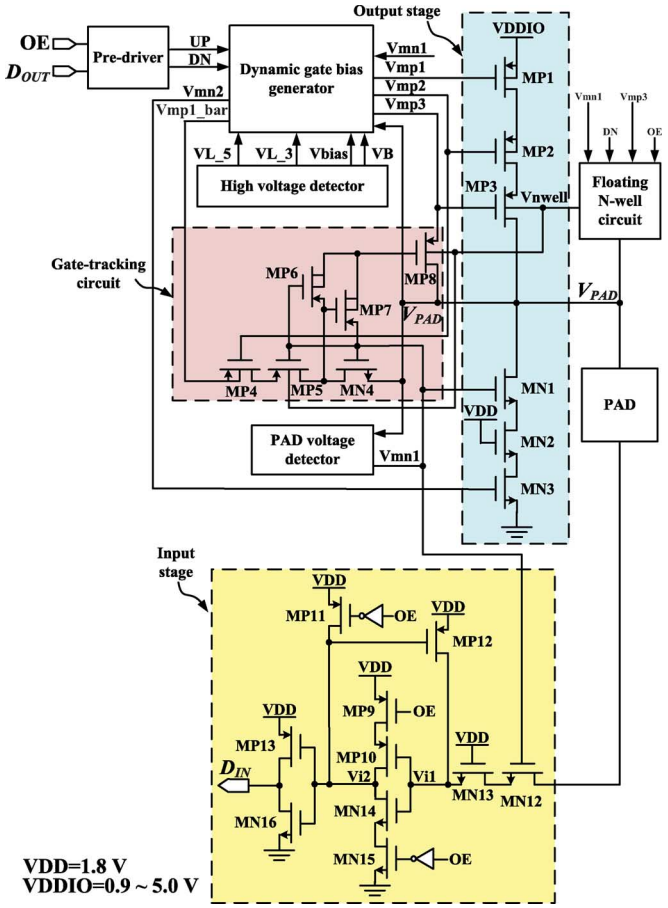

Fig. 1. Schematic diagram of the proposed wide-range bidirectional I/O buffer.

in Output and Input stages. A novel floating N-well circuit as well as a gate-tracking circuit is adopted to eliminate the problems of body effect and the gate-oxide overstress caused by lower and higher voltage signals of Output stage, respectively. Notably, the signal voltage level, VDDIO, can be transmitted or received at 0.9/1.2/1.8/3.3/5.0 V, while the supply voltage of the core circuitry, VDD, is equal to 1.8 V. The detailed descriptions of subcircuits are given in following subsections.

A. Predriver

Fig. 2 shows the schematic of predriver, which is used to predrive and decode digital signals delivered from the core circuitry. OE decides which one of the transmitting mode ($\rm OE = 1.8\ V$) or receiving mode ($\rm OE = 0\ V$) is selected. When the proposed system operates in the Tx mode, the logic state of $V_{\rm PAD}$ is determined by that of $D_{\rm OUT}$, while the logic state of the receiving signal $D_{\rm IN}$ always follows that of $V_{\rm PAD}$.

B. Input Stage

The Input stage circuit is referred to as that of [8]. MN12 and MN13 act as current-limiting resistors to prevent MN14 from the gate-oxide overstress when the voltage at PAD is high, i.e., $V_{\rm PAD} =$ 3.3/5.0 V, in Fig. 1. The detailed operation of Input stage is explained as follows.

In the Rx mode, when $V_{\rm PAD} =$ 5.0/3.3 V, Vi1 is near 1.4 V via MN12 and MN13 to ensure the gate-oxide reliability. Meanwhile, the gate voltage of the transistor MP12 is pulled up to 1.8 V as the logic

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The authors are with Department of Electrical Engineering, National Sun Yat-Sen University, Kaohsiung 80424, Taiwan (e-mail: ccwang@ee.nsysu.edu.tw).

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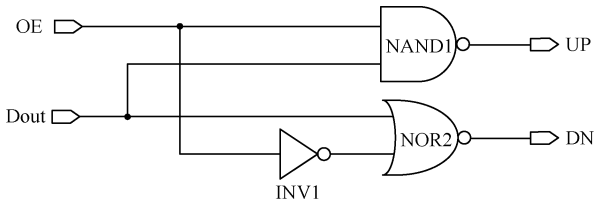

Fig. 2. Schematic of predriver circuit.

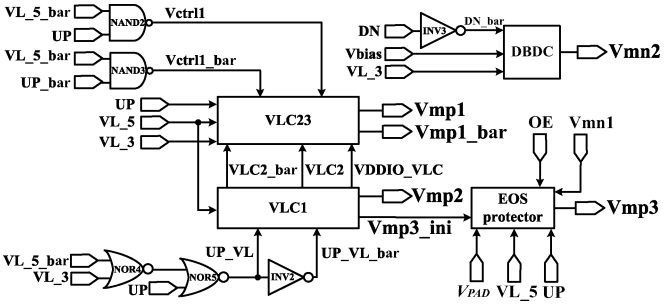

Fig. 3. Schematic diagram of dynamic gate bias generator.

state 1, when $V_{\rm PAD} = 0.9/1.2/1.8/3.3/5.0$ V. At the same time, Vi2 is pulled down to 0 V to turn on MP12 through the invertor composed of MP10 and MN14. Then, Vi1 is pulled up to 1.8 V.

If $\rm OE = 1.8$ V in the Tx mode, both MP9 and MN15 will be off. MP11 is turned on to charge Vi2 to 1.8 V, whereas MP12 is turned off for the elimination of current leakage.

C. Output Stage

Output stage of Fig. 1 is composed of stacked pMOS and nMOS transistors to prevent the effect of gate-oxide overstress. The main functionality of Output stage is to safely transmit and receive the signal voltages from 0.9 to 5.0 V. Their individual gate drives, i.e., Vmp1, Vmp2, Vmp3, Vmn2, are mainly generated by dynamic gate bias generator, which will be described later in the following text.

D. Gate-Tracking Circuit

Gate-tracking circuit which serves as switch controller of the gate voltage, Vmp3, at the output stage, depending on the PAD voltage, is exhibited in Fig. 1. The major benefit of such a circuit design is to prevent from the potential problem of the leakage current path through the transistor MP3 in the Rx mode.

In the Tx mode, when VDDIO is fed with 5.0/3.3 V and the logic state is "1," $\rm Vmp1\_bar = 5.0/3.3$ V as well as $\rm Vmp2 = 3.3/1.8$ V. At the same time, Vmn1 can be biased at 3.3/1.8 V, and then MP8 can be charged to 5.0/3.3V via MP4, MP5, and MP6 to make Vmp3 independent of the PAD voltage so as to avoid activating gate-tracking circuit. In the Rx mode, if $V_{\rm PAD}$ is fed with 5.0/3.3 V and Vmn1 is equal to 3.3/1.8 V, MP7 will not only be turned on, but the gate drive of the transistor MP3 will follow the PAD voltage as well. However, if $V_{\rm PAD}$ is provided with a lower voltage such as 1.8/1.2/0.9/0 V, both Vmn1 and the gate drive of the transistor MP8 will be biased at 1.8 V. Thus, the transistor MP7 will be on, while the transistor MP8 will be off.

E. Dynamic Gate Bias Generator

Dynamic gate bias generator, including two level converters (VLC1 and VLC23), a dynamic bias detection circuit (DBDC), an electrical overstress (EOS) protector, and glue digital logic gates, that is depicted in Fig. 3, plays an important part in compatibility among the subcircuits of the entire I/O, or rather it makes a great impact on the entire system performance especially in its tolerance of the mixed-voltage range. In view of this, the design provides appropriate gate drives for the transistors MP1, MP2, MP3, and MN3 in output stage by means of ensuring the gate-oxide reliability in different scenarios such that the design can achieve the fully wide-range bidirectional performance. The summary of the circuit in the Tx mode $(\rm OE = 1.8\ V)$ is tabulated in Table I.

TABLE I
FUNCTIONAL TABLE OF DYNAMIC GATE BIAS GENERATOR

VDDIO	UP	Vmp1	Vmp2	Vmp3	Vmp1_bar	Vmn2
5.0 V	0 V	3.3 V	3.3 V	3.3 V	5.0 V	0 V
	1.8 V	5.0 V	3.3 V	1.8 V	3.3 V	1.8 V
3.3 V	0 V	1.8 V	1.8 V	1.8 V	3.3 V	0 V
	1.8 V	3.3 V	1.8 V	1.8 V	1.8 V	1.8 V
1.8 V	0 V	0 V	0 V	0 V	1.8 V	0 V
	1.8 V	1.8 V	1.8 V	1.8 V	0 V	1.8 V
1.2 V	0 V	0 V	0 V	0 V	1.2 V	0 V
	1.8 V	1.2 V	1.8 V	1.8 V	0 V	1.2 V
0.9 V	0 V	0 V	0 V	0 V	0.9 V	0 V
	1.8 V	0.9 V	1.8 V	1.8 V	0 V	0.9 V

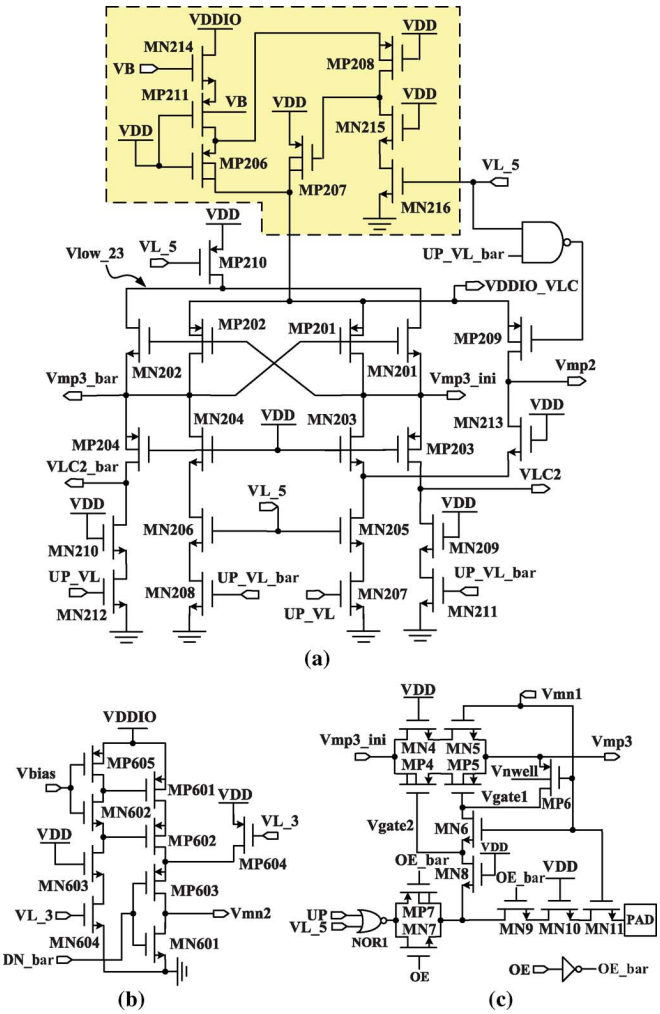

Fig. 4. Schematic diagrams of VLC1, DBDC, and EOS protector.

However, the voltage levels of Vmp1, Vmp2, and Vmp3 in the Rx mode are the same as those when the logic 0 is transmitted in the Tx mode. Besides, a special case is that when the signal is received with 5.0/3.3 V voltage at PAD, Vmp3 is charged toward 5.0/3.3 V through gate-tracking circuit. This can avoid the leakage current caused by the transistor MP3.

1) VLC1: The VLC1 depicted in Fig. 4(a) is used to provide output stage with two biases, Vmp2 and Vmp3, while Vmp3 is generated by EOS protector and Vmp3_ini. Also, this design generates two control signals as well as a voltage level, VLC2, VLC2_bar, and

TABLE II
FUNCTIONAL TABLE OF VLCI

	VDDIO	Logic 0 is at PAD	Logic 1 is at PAD
Vmp2	5.0 V	3.3 V	3.3 V
	3.3 V	1.8 V	1.8 V
	1.8/1.2/0.9 V	1.8 V	0 V
Vmp3_ini	5.0 V	1.8 V	3.3 V
	3.3 V	1.8 V	1.8 V
	1.8/1.2/0.9 V	1.8 V	0 V
VLC2	5.0 V	0 V	3.3 V
VLC2_bar	5.0 V	3.3 V	0 V
VDDIO_VLC	5.0 V	3.3 V	3.3 V
	3.3 V	1.8 V	1.8 V
	1.8/1.2/0.9 V	1.8 V	1.8 V

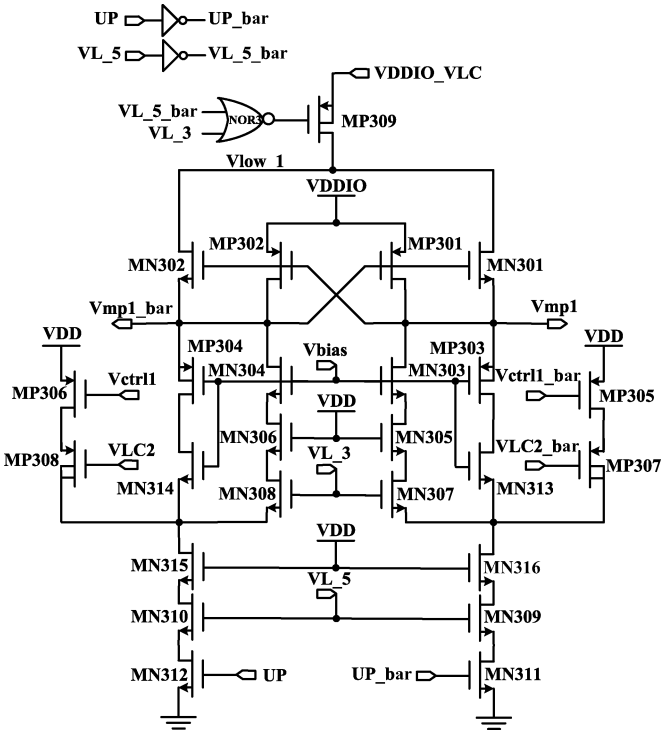

Fig. 5. Schematic diagram of VLC23.

VDDIO_VLC, to VLC23. Besides, the circuit functionality in the part of the dotted line of Fig. 4(a) is to generate a voltage, VDDIO_VLC, varied with VDDIO. Obviously, a $2 \times V_{\rm DD}$ voltage level convertor is implemented through detailed circuit analysis, whose results are summarized in Table II.

2) DBDC and EOS Protector: Both DBDC and EOS protector are shown in Fig. 4(b) and (c), respectively. The function of DBDC is to generate proper biases to output stage based on VDDIO such that it alleviates the problem of duty cycle distortion, especially in the scenario that when VDDIO is lower than 1.8 V, the voltage difference between gate and source of pMOS drops seriously in output stage. In addition, EOS protector constitutes a safeguard among devices against a permanent damage such as the electrical overstress phenomenon of the circuit operated at a high voltage signal. As VDDIO is applied with 5.0 V given $\rm OE = 1.8$ V and $\rm VL\_5 = 0$ V in the Tx mode, Vmp3 will be biased between 3.3 and 5.0 V and sent to Output stage depending on Vmp3_ini. In the same manner, when VDDIO is fed with 3.3/1.8/1.2/0.9 V, the output signal Vmp3 is properly biased from 0 to 1.8 V.

On the contrary, if $V_{\rm PAD} = 5.0/3.3$ V in the Rx mode, Vgate1 and Vgate2 determined by the PAD voltage will be pulled up to 5.0/3.3 V and down to 3.3/2 V, respectively, due to the corresponding signals passing through the Gate-tracking circuit. Similarly, if $V_{\rm PAD} = 1.8/1.2/0.9/0$ V, both Vgate1 and Vgate2 will be charged (discharged) to 1.4/1.2/0.9/0 V.

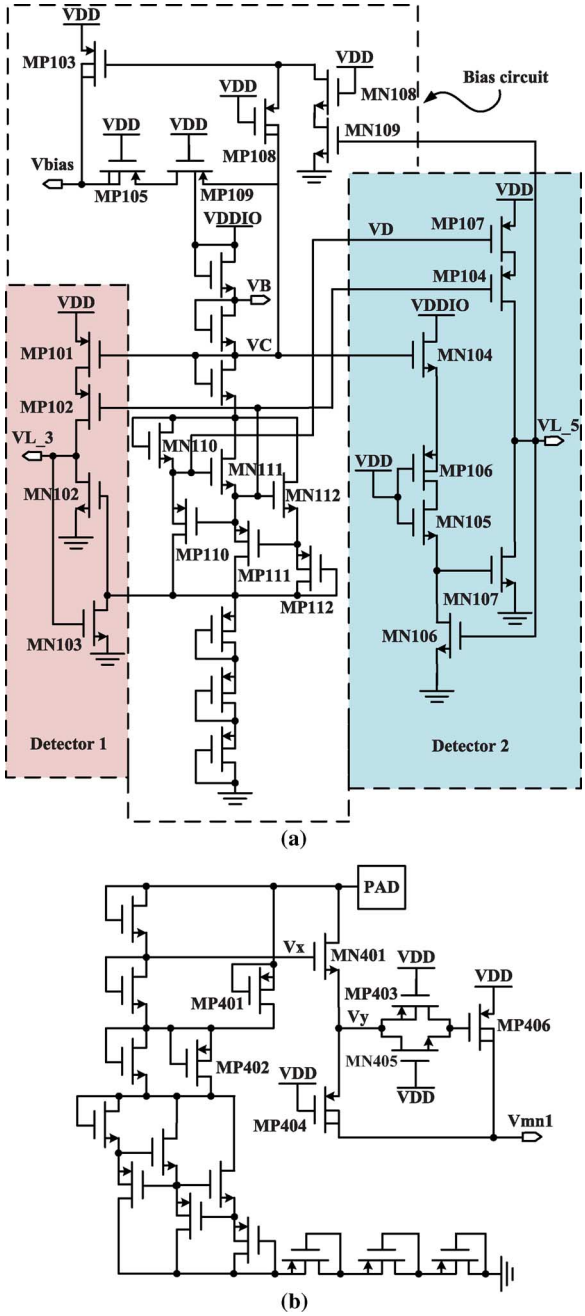

Fig. 6. Schematic diagrams of high voltage detector and PAD voltage detector.

3) VLC23: As shown in Fig. 5, VLC23 generates two critical biases, Vmp1 and Vmp1_bar, to output stage and gate-tracking circuit, whose functionality is to effectively generate a higher voltage such as $3 \times V_{\rm DD}$ level, namely $3 \times V_{\rm DD}$ voltage level convertor. After completely analyzing the operation of the above items depending on VDDIO, we attain the same results as the first, third, and sixth columns in Table I.

F. High Voltage Detector

High voltage detector is composed of a bias circuit and two detector circuits, Detector 1 and Detector 2, to pass the four output signals on, i.e., VB, Vbias, VL_5, and VL_3, of Fig. 6(a) with a closed-loop structure such that not only do all transistors enter the subthreshold region, but attain very low static current as well. The scheme has the capability

TABLE III
FUNCTIONAL TABLE OF HIGH VOLTAGE DETECTOR

VDDIO	VB	Vbias	VL_5	VL_3
5.0 V	4.3 V	3.3 V	0 V	0 V
3.3 V	2.6 V	1.8 V	1.8 V	0 V
1.8 V	1.1 V	1.8 V	1.8 V	1.8 V
1.2 V	0.5 V	1.8 V	1.8 V	1.8 V
0.9 V	0.2 V	1.8 V	1.8 V	1.8 V

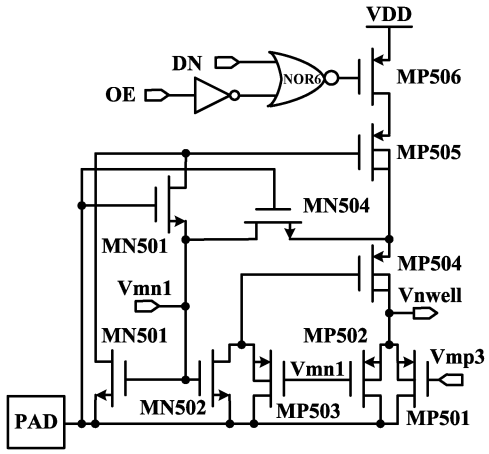

Fig. 7. Schematic diagram of floating N-well circuit.

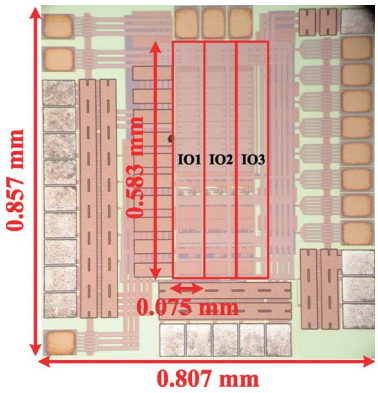

Fig. 8. Die photo of the proposed high-speed I/O buffer.

of detecting if VDDIO is higher than 1.8 or 3.3 V as well as of generating two corresponding signals, VL_5 and VL_3, to dynamic gate bias generator. The results of the circuit analysis are briefly summarized in Table III.

G. PAD Voltage Detector

Consider a simplified structure of the PAD voltage detector and refer to Fig. 6(b). Such a major role does this circuit play that it will effectively control the gate drive of MN1, Vmn1, of Output stage, depending on the PAD voltage. Thus, after analyzing this circuit, we give a brief summary that Vmn1 is operated at 3.3/1.8/1.8/1.8/1.8/1.8 V for the PAD voltages with 5.0/3.3/1.8/1.2/0.9/0 V, respectively.

H. Floating N-Well Circuit

Last but not least, the floating N-well circuit depicted in Fig. 7 is used to achieve high speed performance. Specifically, this circuit functions as a bulk bias generator for MP3 in Fig. 1 and Vnwell to output stage such that it may not merely avoid the undesired leakage current through the parasitic P+/N-well diode, but also prevent the occurrence of the body effect generated when Output stage is operating in the Tx mode.

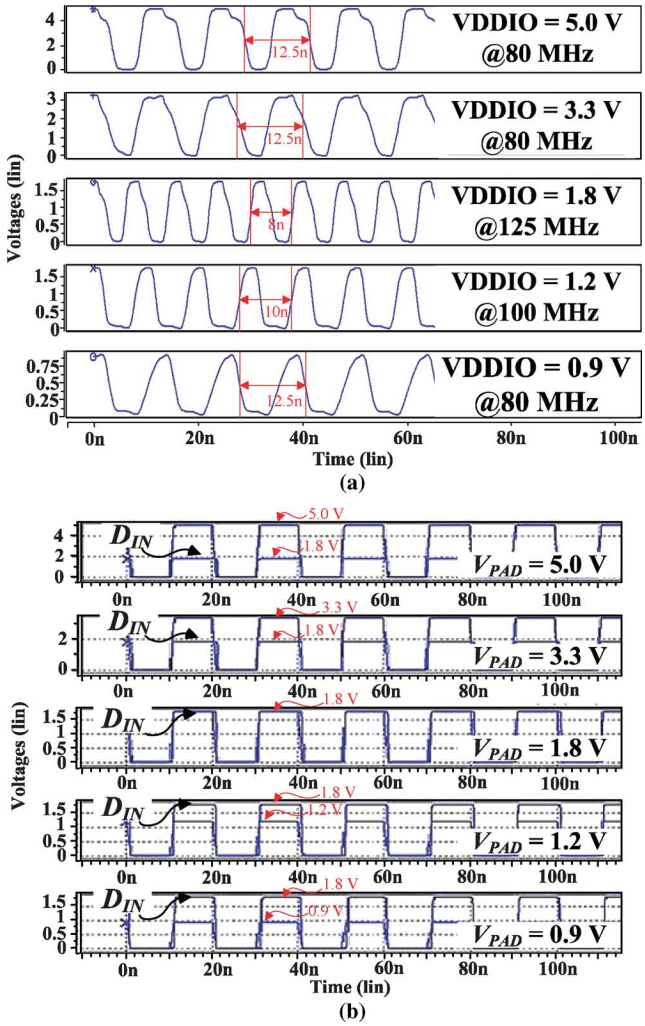

Fig. 9. (a) Maximum data rate with different VDDIO in the Tx mode and (b) V_{PAD} and D_{IN} with different V_{PAD} in the Rx mode.

TABLE IV
COMPARISON WITH SEVERAL PRIOR WORKS

	[6]	[2]	[7]	[8]	Ours
# of voltage modes	2	1	3	5	5
Max. operating voltage	3VDD	3.3VDD	1.5VDD	3VDD	3VDD
Min. operating voltage	VDD	3.3VDD	0.54VDD	0.5VDD	0.5VDD
Normal voltage (VDD)	1.0 V	1.0 V	3.3 V	1.8 V	1.8 V
Process (μm)	0.13	0.13	0.35	0.18	0.18
Max. Speed (MHz)	133	133	80	50	125
Area (mm^2)	0.011	0.032	0.034	0.041	0.044
Normalization of Area (mm^2)	0.011	0.032	0.004	0.021	0.023
Year	2006	2007	2009	2009	2010

Next, the analysis proceeds in detail as follows. When a lower voltage signals, i.e., 0.9/1.2/1.8 V, is applied in the Tx mode, Vmp3 is equal to 0 V and the gate voltage of the transistor MP506 is applied at 1.8 V to turn off for reducing the leakage current. However, when the logic 0 is transmitted, both Vmn1 and Vmp3 are biased at 1.8 V to shut MP501 and MP502 off. Then, Vnwell will be charged toward 1.8 V via MP506, MP505, and MP504. On the contrary, if the PAD voltage is applied at a higher level such as 5.0/3.3 V, Vmn1 will be biased at 3.3/1.8 V, respectively. Meanwhile, both MP502 and MP503 will be on such that Vnwell will be pulled up to 5.0/3.3 V, whereas the transistor MP504 is off to prevent the phenomenon as already mentioned earlier.

As the PAD voltage is driven by 0/0.9/1.2/1.8 V in the Rx mode, Vmn1 and Vmp3 both equal to 1.8 V to turn MP501 and MP503 off. Moreover, Vnwell is charged to 1.8 V via MP506, MP505, and MP504.

III. Implementation and Measurement

To demonstrate the performance, we utilize only thin-oxide devices in a 0.18 μm typical CMOS technology to implement the proposed design. The die photo of our I/O buffer is shown in Fig. 8. The maximum data rates with different VDDIO are shown in Fig. 9(a) in the Tx mode. When VDDIO is 5.0/3.3/1.8/1.2/0.9 V, the maximum speed is found to be 80/80/125/100/80 MHz, respectively, with a given capacitive load of 10 pF. Next, given different $V_{\rm PAD}$ in the Rx mode, the waveforms of both $V_{\rm PAD}$ and $D_{\rm IN}$ in Fig. 9(b) show that all of $D_{\rm IN}$ voltage levels are switched to 1.8 V. The proposed I/O buffer does not resolve the ground-bounce effect completely. However, it can be reduced by sizing transistors properly. Finally, the performance of our scheme compared with that of prior I/O buffers is depicted in Table IV and our static power consumption is estimated to 17 μW in the worst case.

IV. Conclusion

Implementation results indicate that our scheme without utilizing thick-oxide technology not only can transmit and receive the signals which are tolerant of different voltages from $(1/2) \times V_{\rm DD}$ to $3 \times V_{\rm DD}$, but also can attain the highest data rate, 125 MHz, by using an innovative Floating N-well circuit with a 1.8 V power supply. What is more, the intrinsic drawbacks of body effect, gate-oxide overstress, and leakage current are all obviated.

Acknowledgment

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A Parameterized Programmable MIMO Decoding Architecture With a Scalable Instruction Set and Compiler

Karim Mohammed, M. I. A. Mohamed, and Babak Daneshrad

***Abstract*—We present a novel multiple-input multiple-output (MIMO) decoder accelerator and its associated integrated design environment. The accelerator architecture allows tradeoffs in decoding algorithm, antenna configuration, modulation scheme, and bandwidth at run-time via user programming. The accelerator delivers an improvement over a general purpose digital signal processor (DSP) reaching three orders of magnitude for matrix processing and linear MIMO decoding. The hardware architecture is user-configurable through ten independently set parameters. The parameterization allows independent control over the size and structure of the processing core as well as the structure, size, and access scheme of data memory. We provide a custom high level script and a scalable machine level instruction set and compiler. The elements of hardware configuration and programmability are combined in a user-friendly design flow that takes the MIMO decoder designer from simulation to hardware with dedicated-hardware-like performance in no time.**

***Index Terms*—Application-specific processor, configurable multiple-input-multiple-output (MIMO) decoder, MIMO accelerator.**

I. Introduction

Multiple-input–multiple-output (MIMO) processing and orthogonal frequency division multiplexing (OFDM) are two dominant technologies in emerging wireless communications systems. MIMO transmission increases the capacity and reliability of a wireless system without increasing its bandwidth. OFDM divides a wideband channel into multiple narrowband subchannels via a computationally efficient fast Fourier transform (FFT) operation, but it requires identical baseband processing for each of the subchannels. Multiple standards rely on MIMO-OFDM to provide high spectral efficiency and to enable broadband communication.

The MIMO decoder is one of the most complex blocks in a MIMO transceiver; it inverts a channel matrix with a low-latency requirement for each subcarrier. A MIMO decoder design process for a certain application is hard and time consuming. This motivates the need for a programmable accelerator block to implement the MIMO decoder and a fast and easy application-driven MIMO decoder design flow.

MIMO decoders are traditionally designed using dedicated datapaths [1]–[3] for high throughput applications. When throughput requirements are sufficiently low, they can be implemented on microprocessor, digital signal processor (DSP), or mixed platforms for programmable applications [4]. Several reconfigurable MIMO decoders have been reported in the literature such as [5], [6]. These decoders apply a fixed algorithm and provide enough hardware for the most complex configuration it performs. The other configurations use subsets of the decoder hardware. A programmable MIMO detector is presented in [7] using a software-driven processor that employs several general-purpose floating-point processing units. It is general to the extent of being

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K. Mohammed was with the University of California, Los Angeles, CA 90095 USA. He is now with Cairo University, Giza 12613, Egypt (e-mail: kabbas@ee.ucla.edu).

M. I. A. Mohamed and B. Daneshrad are with the University of California, Los Angeles, CA 90095 USA (e-mail: mismail@ee.ucla.edu; babak@ee.ucla.edu).

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