A Single-Chip 60-V Bulk Charger for Series Li-Ion Batteries With Smooth Charge-Mode Transition

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***Abstract*—In this paper, a single-chip 60-V battery charger prototype is presented. The newly proposed charge mode transition can ensure smooth transitions between incremental current (IC), constant current (CC), and constant voltage (CV) modes. The charger sources a current of 136 mA in CC mode and has an efficiency up to 92% during the charging sequence. Intentional saturation of both the IC and CV regulation loops ensure the stability of the charger throughout the charging sequence. Bonding PAD designed to remove the constraints on the aspect ratio of input transistors as a prevention of antenna effect is also disclosed. The proposed design has been implemented on silicon using the TSMC 0.25 μm 1-poly 3-metal bipolar-CMOS-DMOS (BCD) 60-V process.**

***Index Terms*—Antenna effect, charger, constant current, constant voltage, high voltage integrated circuit, incremental current.**

I. Introduction

GLOBAL warming due to greenhouse gas emission such as CO_2 and CH_4 has attracted very much attention of governments and organizations worldwide. To respond to the exigent call for greener means of transportation and miscellaneous collection of applications, the development of vehicles and other mobile systems electrically powered by batteries are beginning to gain momentum. Until now, a great majority of power management systems that require at least tens of volts must be implemented using discrete power electronic devices. The incapability of MOS transistors in a modern integrated circuit process to sustain high voltages render the implementation of high voltage (HV) power management circuits using an integrated system-on-chip (SoC) solution impossible. For such reasons, integrated power management solutions are limited to particular applications such as smart phones, tablet PCs, digital cameras, etc., where only a low supply voltage is required.

To overcome this limitation, certain HV processes with vertical double-diffused MOS (VDMOS) devices have been developed to meet the demand of HV applications [1]. However, the channel length of the transistors implemented using these processes does not depend on the resolution of the photolithography. Instead, it is controlled by the lateral spreads of phosphorus and boron diffusions. The non-planar characteristics make integration of these devices into standard digital CMOS processes very difficult [2]. An alternative approach around this problem is to use lateral double-diffused MOS (LDMOS) transistors. These devices have lateral drift extension, which is similar to transistors in a standard digital CMOS process. The integration of such devices and the standard digital CMOS process has been reported in [3]. After almost a decade of advancement in semiconductor technologies, mass production using such a process, like the TSMC 0.25 μm bipolar-CMOS-DMOS (BCD) HV process [4] used to carry out the design, is now feasible. This process offers a variety of devices to meet different requirements of various applications [5]. The design of low voltage analog circuits as well as cell-based standard digital library designs can be carried out using 0.25 μm standard CMOS. High performance analog circuits operating at a supply voltage of 5 V can be designed using 0.5 μm standard CMOS. Asymmetrical N-type and P-type LDMOS transistors that can support up to 60 V are adequate for HV applications. It is important to highlight that the maximum sustainable voltages between the three terminals are not equivalent. As depicted in Fig. 1, the gate-drain and drain-source voltages can endure up to 60 V, but the maximum voltage between gate and source is strictly limited to 5 V only.

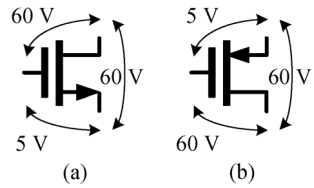

Fig. 1. The maximum sustainable voltages between different terminals of: (a) N-type, and (b) P-type LDMOS transistors.

Batteries are an essential component of most electrically powered environment friendly applications. Given the TSMC 0.25 μm bipolar-CMOS-DMOS (BCD) HV process, high voltage battery chargers capable of charging series connected batteries can be built using only integrated circuits and passive components. Basically, battery charger topologies used to charge series connected batteries can be sorted into three categories. These topologies include a bulk charger that charge all the batteries, a series of small chargers that independently charge their respective batteries, or a combination of both, as illustrated in Fig. 2 [6]. To take full advantage of the HV tolerance offered by this process, the bulk charger topology is

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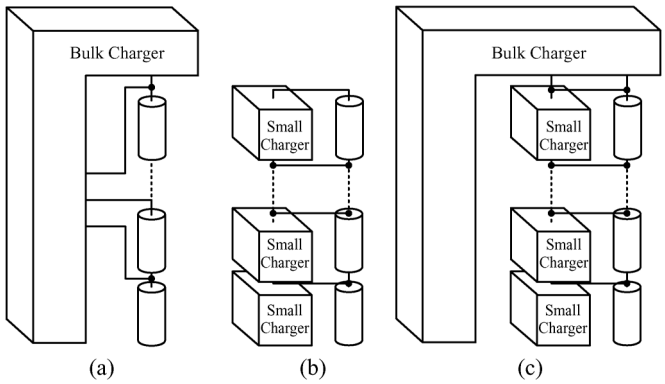

Fig. 2. (a) Bulk charger. (b) Small chargers. (c) Combination of both.

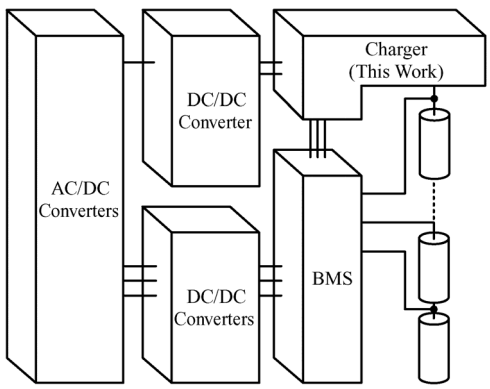

Fig. 3. Architecture of the battery charger.

selected for exemplification. Although balanced charging by the bulk charger is not inherently achieved without a series of small chargers, it can be easily enhanced with the inclusion of a battery management system (BMS) chip which actively balance and redistribute energy among the batteries. A complete embodiment of the system shown in Fig. 3 would also take advantage of ac/dc and dc/dc converters to provide a variable voltage corresponding to the battery voltage to the charger so that high charging efficiency can be achieved throughout the charging sequence [7].

This study is mainly focused on the design of the bulk charger, which is made capable of operating in both constant current (CC) mode and constant voltage (CV) mode. The bulk charger also supports a newly proposed incremental current (IC) mode, which is dedicated for economic integrated circuit packaging where a high parasitic inductance is included in the charging path. Section II serves as a quick introduction to the characteristics and limitation of the devices available to the HV process used to carry out this design. Conventional charging strategies and the associated problems regarding mode transition is also elucidated. Our system embodiment and the proposed charging sequence are covered in Section III. In Section IV, the analysis of circuits that is used to implement the bulk charger is presented. Notably, a solution that removes the stringent transistor sizing requirement imposed by the prevention of antenna effect is also revealed in this section. Experimental results are evaluated and compared with simulation results in Section IV.

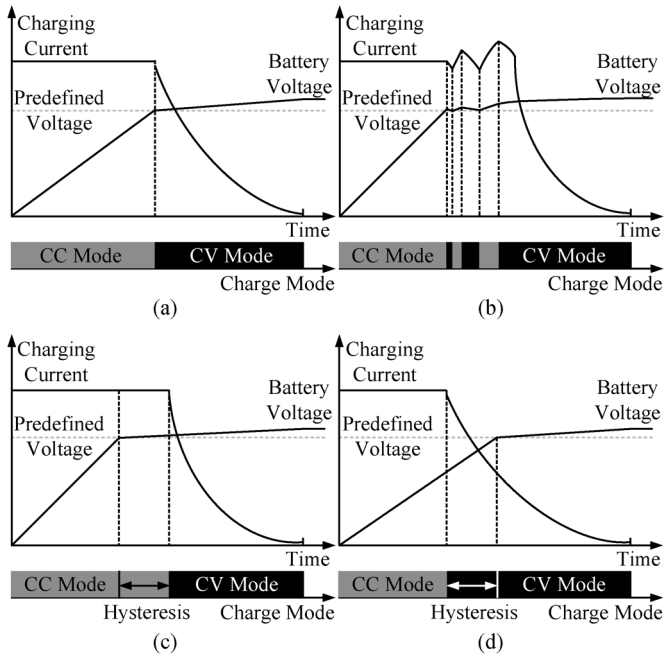

Fig. 4. (a) Current and voltage characteristics of an ideal CC/CV charger. (b) An unstable charger with oscillation between CC and CV modes. (c) A charger with positive hysteresis. (d) Negative hysteresis.

II. Comparison of Charging Strategies

When the voltage of the battery is low, a conventional battery charger starts the charging sequence by sourcing a regulated current to the battery, which is well known as the constant current (CC) mode. When the battery voltage rises, its internal ESR also increases. The battery charger is then switched into the constant voltage (CV) mode as soon as the battery voltage reaches a predefined level, where the charging voltage of the battery is regulated. When the battery voltage reaches the designated voltage level, the charging sequence is terminated. This charging strategy depicted in Fig. 4(a) is popularly regarded as the constant-current/constant-voltage (CC/CV) technique, which has been widely used in prior literature [7], [9]–[22]. However, straightforward implementation of the CC/CV technique using a voltage comparator can result in a potential stability problem during charge mode transition. As conceptually shown in Fig. 4(b), the charger switches from CC mode to CV mode as the feedback voltage from the battery becomes larger than the predefined reference voltage. An abrupt change of the charging current on the parasitic resistance causes a sudden voltage drop on the charging path from the charger to the battery, which in turn causes the sensed feedback voltage to drop. Consequently, the predefined reference voltage has a larger voltage value in comparison, and the charger is switched back to CC mode [10]. This kind of back-and-forth transitions can occur for an indefinite number of times during the entire charging sequence.

An apparent solution is to add hysteresis to the comparator to squelch the unstable rapid transitions between CC and CV modes, as demonstrated in Fig. 4(c) and (d). However, it is not easy to define an appropriate range of the hysteresis. Assume that the feedback voltage is connected to the positive node of

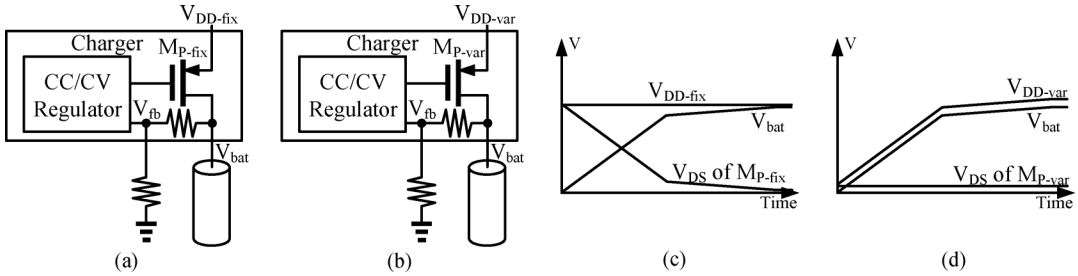

Fig. 5. Chargers with: (a) fixed and (b) variable supply voltage, and their conceptual voltages throughout the charge sequence (c), (d).

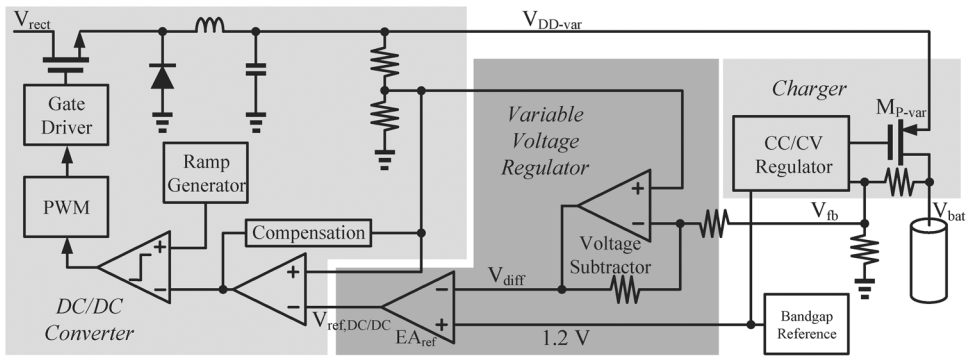

Fig. 6. A dc/dc converter controlled by the variable voltage regulator provides an appropriate variable supply voltage to a charger.

the comparator and the predefined voltage is coupled to the negative input of the comparator. Potential overheating of the battery may occur if the positive hysteresis range is made too large, delaying the entrance to CV mode. [12]. By contrast, if the negative hysteresis is used and the range is made too large, it will cause the battery charger to enter CV mode prematurely. Finally, if the hysteresis range is made too small, the rapid oscillation may still occur [10].

In Fig. 5(a), a charger consisting of a power MOS $\mathrm{M_{P-fix}}$ and a CC/CV regulator starts its charging sequence in CC mode. Since the battery is uncharged, the voltage node at $\mathrm{V_{bat}}$ is at a low voltage value and the drop-out voltage $\mathrm{V_{DS}}$ across the transistor $\mathrm{M_{P-fix}}$ is as high as the voltage difference between $\mathrm{V_{DD-fix}}$ and $\mathrm{V_{bat}}$. $\mathrm{V_{DS}}$ will become gradually smaller as the battery is charged and $\mathrm{V_{bat}}$ increases. However, since the charger charges the battery by regulating a high current to the battery in CC mode, the charging current will also flow directly through $\mathrm{M_{P-fix}}$ and cause a significant power loss on $\mathrm{M_{P-fix}}$. Thus, such chargers are only capable of providing an inherently low charging efficiency. Heat dissipation can be another serious issue as well. The charger has different cooling requirement throughout the charging sequence,which must be accounted for the worst case when most power are dissipated across the transistor $\mathrm{M_{P-fix}}$. Therefore, economic packaging, e.g., side-brazed dual in-line packages, cannot meet the cooling constraint imposed by such chargers. By contrast, the charger shown in Fig. 5(b) is supplied by a variable supply voltage, $\mathrm{V_{DD-var}}$. This supply voltage is intended to track and provide a voltage slightly higher than $\mathrm{V_{bat}}$. Hence, the drop-out voltage $\mathrm{V_{DS}}$ across the transistor $\mathrm{M_{P-fix}}$ is maintained at a predefined value such that the charging efficiency is significantly improved in the CC mode [7], [9], [12], [17]. The cooling requirement of such chargers in CC mode is also made less stringent as well. The main overhead of implementing such a charger would be the need for an additional dc/dc converter, and the overall efficiency will also be affected by the efficiency of the dc/dc converter.

III. Proposed Charging Strategy

A. Embodiment of the Battery Charging Solution

As depicted in Fig. 2, a complete battery charging system usually include a BMS, ac/dc converters, dc/dc converters, and a bulk charger [6]. The BMS is in charge of balancing the serially connected Li-ion batteries. The ac/dc converter is used to provide a rectified dc voltage, denoting as $\mathrm{V_{rect}}$ in Fig. 6, to the dc/dc converters. DC/DC converters with fixed output voltage are used to provide power for both the controller circuits of the charger and the BMS, and an independent dc/dc converter (depicted in Fig. 6) is used to provide a variable voltage, $\mathrm{V_{DD-var}}$, for the charger.

The generation of a variable voltage can be understood by inspecting Fig. 6. First of all, a voltage subtractor is used to subtract the difference between the feedback voltage of the charger and dc/dc converter to generate a value $\mathrm{V_{diff}}$, which represents the voltage difference between $\mathrm{V_{DD-var}}$ and $\mathrm{V_{bat}}$. An error amplifier, $\mathrm{EA_{ref}}$, regulates $\mathrm{V_{diff}}$ to a bandgap reference voltage value of 1.2 V by adjusting $\mathrm{V_{ref,dc/dc}}$, which serves as a variable reference voltage for the dc/dc converter. Finally, by using pulse width modulation (or any other appropriate modulation), the variable voltage is generated. Since charging operation is considerably slower than the dynamic response of the dc/dc converter, it would be unnecessary for the dc/dc converter to be designed with fast reference tracking capability.

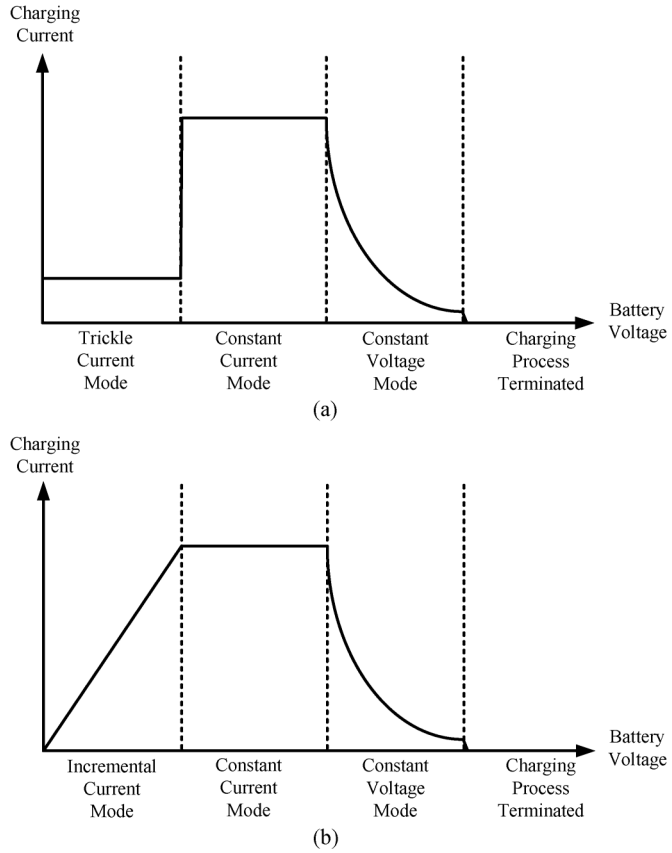

Fig. 7. The relationship of charging current against battery voltage for a battery charger with: (a) trickle current mode, and (b) incremental current mode. Note that the XY axis of this figure differs from that of Fig. 5.

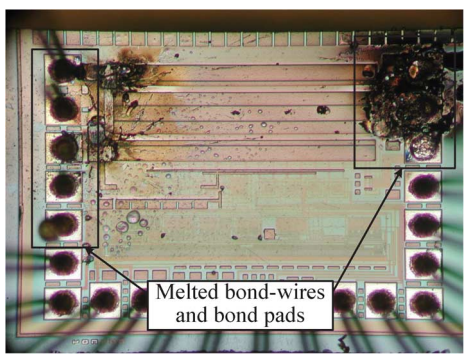

Fig. 8. The aftermath of inductive kickback. Both the bond-wires and the bond pads are permanently damaged.

B. Incremental Current, Constant Current, and Constant Voltage Modes

During the initial charging sequence, it may be inappropriate to charge deeply uncharged batteries with a high current. The trickle current (TC) mode [7] can resolve this problem by sourcing a smaller current to the battery, and switch to CC mode when the battery voltage reaches a predefined value, as shown in Fig. 7(a). In practical scenarios, the charger circuit fabricated on a chip must be packaged, thereby introducing parasitic inductance on the bond-wires with a value ranging from 1 nH to 3 nH on the charging path. The parasitic inductance depends on the length of the bond-wires, which cannot be easily estimated before the chip is packaged. If both the parasitic inductance and the charge current are large enough, a sudden switch from the TC mode to the CC mode will result in an inductive kickback, melting both the bond-wires and the connected pads, as shown in Fig. 9. To prevent such catastrophes, the TC mode is modified into the incremental current (IC) mode, as shown in Fig. 7(b). The charging current becomes a function of the battery voltage. More specifically, the charging current increases gradually as the battery voltage increases. However, this charging current does not increase unlimitedly. It is clamped at a predefined value, which the charger enters the CC mode without a discontinuous transition with respect to the charging current.

IV. Circuit Implementation

A. Constant Voltage Loop and Diode-Based Constant Current Clamp

As depicted earlier in Fig. 5, there can be problems switching from CC and CV mode. Apparently, smooth charge mode transition between CC to CV modes is essential to the stability of a charger. To elegantly resolve this problem, the CV regulating loop should be able to clamp the maximum output charging current. In other words, the CC and CV feedback loops are combined into one, which has been reported in [12]. As shown in Fig. 9(a), this scheme consists of a linear dropout regulator (LDO)-like constant voltage controller and a series of diodes D_1 to D_N, where N is the number of diodes. In CV mode, the charger behaves analogously to a typical LDO. An error amplifier, $\mathrm{EA}_{\mathrm{cvfb}}$, is used to generate an error voltage, V_{cv}, based on the difference of the shunt-feedback battery voltage V_{cvfb} and the reference voltage V_{cvref}. V_{cvref} is responsible of driving the cascaded level shifter which in turn biases the power MOS $\mathrm{M}_{\mathrm{Power}}$ is driven by the level shifter so that an appropriate amount of current is regulated into the battery.

In situations when V_{cvfb} is far lower than the predefined V_{cvref}, V_{cv} is pulled up close to the supply voltage of $\mathrm{EA}_{\mathrm{cvfb}}$, and $\mathrm{M}_{\mathrm{hvcs}}$ will attempt to pull the gate of $\mathrm{M}_{\mathrm{Power}}$ all the way to ground. However, since $\mathrm{M}_{\mathrm{hvcs}}$ is designed with the minimum width and long length in dimension, and it is also source-degenerated with $\mathrm{R}_{\mathrm{cvs}}$, its current sinking ability is limited. Hence, the diodes D_1 to D_N will clamp the gate of $\mathrm{M}_{\mathrm{Power}}$ at a value of V_{Clamp} lower than $\mathrm{VDD}_{\mathrm{HV}}$. This can ensure that the maximum value of I_{Charge} is limited to a finite value governed by

$$\begin{aligned} I_{\mathrm{Charge}} &= \frac{1}{2}K_p'\frac{W}{L}(V_{\mathrm{Clamp}} - V_{\mathrm{thp}})^2 \\ &= \frac{1}{2}K_p'\frac{W}{L}(N \times V_{Don} - V_{\mathrm{thp}})^2. \end{aligned} \tag{1}$$

As revealed in (1), the absolute resistance value of $\mathrm{R}_{\mathrm{cvs}}$ does not affect the charging current, as long as the diodes can be turned on. The sensitivity of the charging current with respect to the voltage variation over the diode string is given as follows:

$$\begin{aligned} S_{N\times V_{\mathrm{Don}}-V_{\mathrm{thp}}}^{I_{\mathrm{Charge}}} &= \frac{\partial I_{\mathrm{Charge}}/I_{\mathrm{Charge}}}{\partial(N \times V_{\mathrm{Don}} - V_{\mathrm{thp}})/(N \times V_{\mathrm{Don}} - V_{\mathrm{thp}})} \\ &= \frac{\partial I_{\mathrm{Charge}}}{\partial(N \times V_{\mathrm{Don}} - V_{\mathrm{thp}})} \times \frac{N \times V_{\mathrm{Don}} - V_{\mathrm{thp}}}{I_{\mathrm{Charge}}} \\ &= \frac{K_p'\frac{W}{L}(N \times V_{\mathrm{Don}} - V_{\mathrm{thp}})^2}{I_{\mathrm{Charge}}} \\ &= 2. \end{aligned} \tag{2}$$

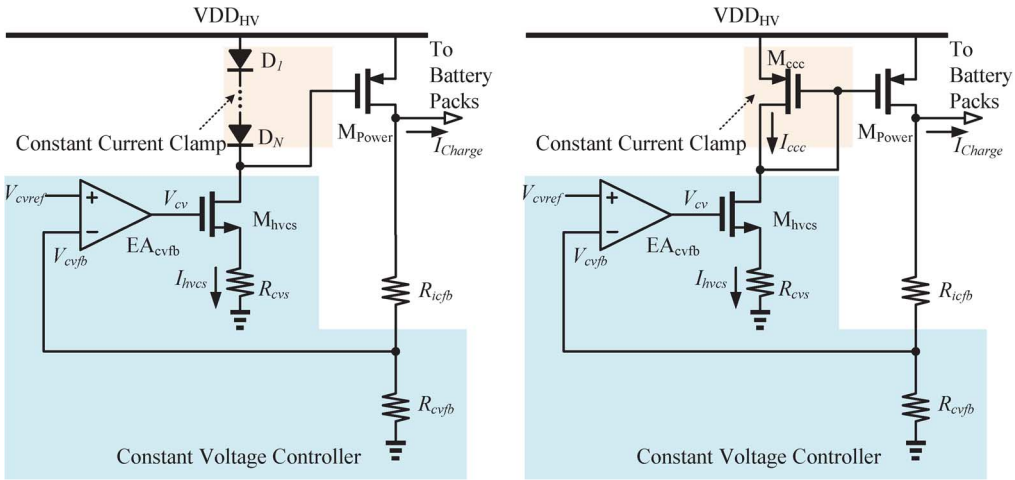

Fig. 9. (a) The constant voltage controller with diode-based constant current clamp [12]. (b) The constant voltage controller with diode-connected load as constant current clamp.

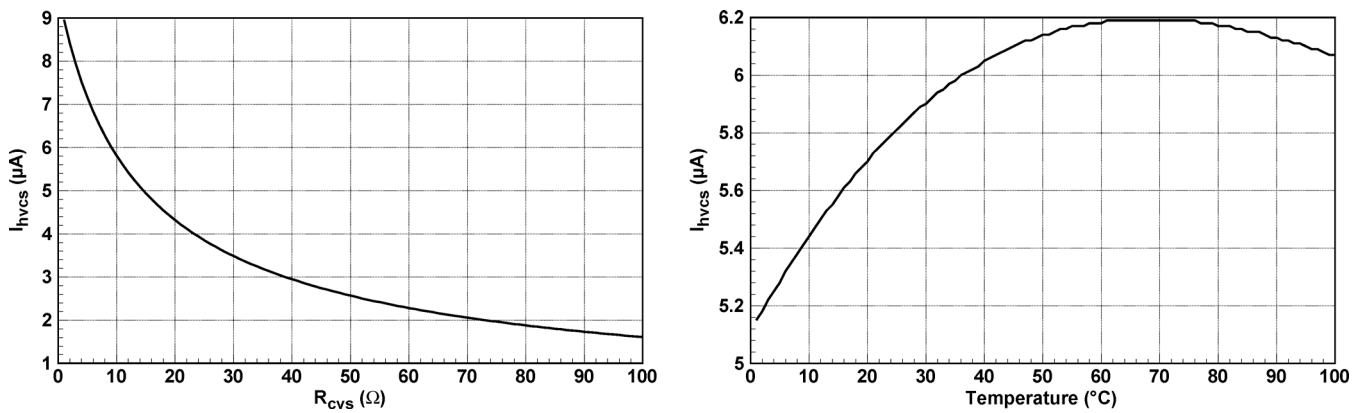

Fig. 10. (a) The nonlinear relationship between $I_{\rm hvcs}$ and $R_{\rm cvs}$. (b) The nonlinear relationship between $I_{\rm hvcs}$ and temperature.

This indicates that the charging current $I_{\rm Charge}$ is sensitive to both $V_{\rm Clamp}$ and $V_{\rm thp}$ by a factor of 2. For example, if $V_{\rm Clamp} - V_{\rm thp}$ is only 80% of the desired value (20% variation), $I_{\rm Charge}$ becomes 64% of the anticipated maximum charging current (36% variation). Hence, the actual charging current will deviate greatly from simulation results. This also explains the low charging current and, consequently, the low efficiency of the charger proposed in [12].

B. Constant Voltage Loop and Diode-Connected Load as Constant Current Clamp

To avoid such an undesired deviation, the voltage clamp should be made adjustable after the charger has been fabricated on silicon to account for process variation. Instead of placing serially connected diodes to clamp the voltage, a diode-connected power PMOS $\rm M_{ccc}$ is used, as shown in Fig. 9(b). From the following equations:

$$V_{\rm cv} = V_{\rm gs,hvcs} + I_{\rm hvcs} \times R_{\rm cvs} = 5 \tag{3}$$

$$I_{\rm ccc} = I_{\rm hvcs} = \frac{1}{2} K_n' \left(\frac{W}{L}\right) (V_{\rm gs,hvcs} - V_{\rm thn})^2 \tag{4}$$

we attain

$$V_{\rm Clamp} = \sqrt{\frac{10 - 2V_{\rm gs,hvcs}}{R_{\rm cvs} \times K_p'}} - V_{\rm thp} \tag{5}$$

where $V_{\rm gs,hvcs}$ is the gate-source voltage of $\rm M_{hvcs}$, $V_{\rm cv}$ is the gate voltage of $\rm M_{hvcs}$ pulled up to the supply voltage value of 5 V, and 10 is two times of the 5 V supply voltage. Evidently, the maximum gate-source voltage $V_{\rm Clamp}$ of $\rm M_{ccc}$ and $\rm M_{Power}$ is no longer a fixed value, but an adjustable voltage determined by the resistance value of $R_{\rm cvs}$. The nonlinear relationship between $I_{\rm hvcs}$ and $R_{\rm cvs}$ is plotted in Fig. 10(a).

This implementation can also be interpreted as a current mirror copying the current that flows through $R_{\rm cvs}$, multiplying the current by the aspect ratio of $\rm M_{Power}$ vs. $\rm M_{ccc}$, and generating $I_{\rm Charge}$ to charge the battery.

If an npn transistor is used in the place of $\rm M_{hvcs}$, this equation becomes

$$V_{\rm Clamp} = \sqrt{\frac{10 - 2V_{be}}{R_{\rm cvs} \times K_p'}} - V_{\rm thp} \approx \sqrt{\frac{8.6}{R_{\rm cvs} \times K_p'}} - V_{\rm thp}. \tag{6}$$

Since $\rm M_{Power}$ also shares the same $V_{\rm thp}$ and K_p' with $\rm M_{ccc}$, $I_{\rm Charge}$ becomes a clearly defined value with respect to $R_{\rm cvs}$. Unfortunately, with the absence of an npn transistor with high β value in this process, this solution is currently unavailable.

Note that the resistance of $R_{\rm cvs}$ is also a function of temperature, making $I_{\rm Charge}$ temperature-dependent. The resistor value can be generally approximated by [23]

$$R(T) = R_0 \times \{1 + {\rm TC1}\ \Delta T + {\rm TC2}\ \Delta T^2\} \tag{7}$$

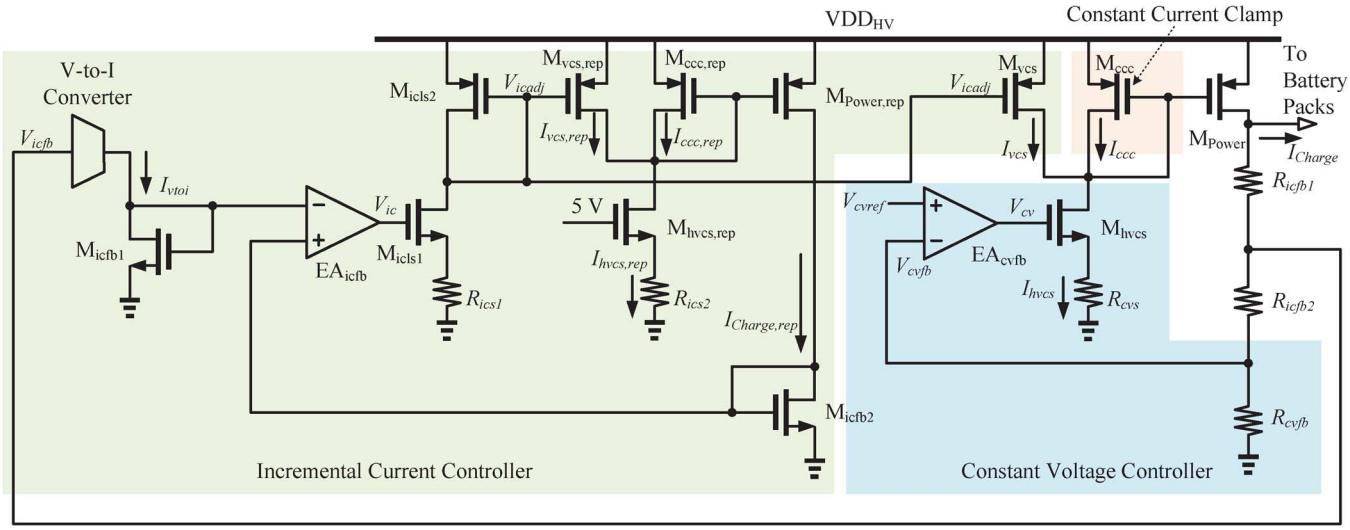

Fig. 11. The incremental current controller augmented to the constant voltage controller with diode-connected load as constant current clamp.

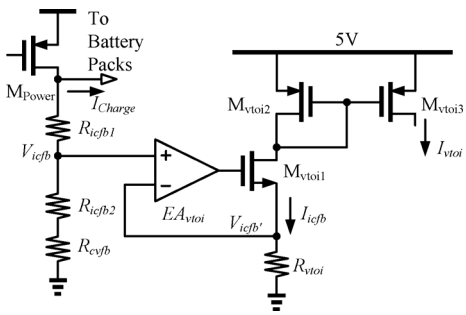

Fig. 12. The schematic of the V-to-I converter.

where TC1 and TC2 are temperature coefficients, R_0 is the resistance measured at room temperature, and ΔT is the difference between the temperature with the room temperature 25 °C. The nonlinear relationship between of $I_{\rm Charge}$ and temperature is plotted in Fig. 10(b) using a resistor of 10 kΩ with coefficients $\mathrm{TC1} = 10^{-2}$ and $\mathrm{TC2} = 10^{-4}$ as $R_{\rm cvs}$.

C. Incremental Current Loop

Fig. 11 shows the schematic of the incremental current controller augmented to the original CV controller. The V-to-I converter is responsible of generating a reference current, $I_{\rm vtoi}$, corresponding to the contemporaneous battery voltage. As depicted in Fig. 12, the virtual-short characteristic of the error amplifier $\mathrm{EA_{vtoi}}$ causes the feedback voltage $V_{\rm icfb}$ to be copied to $V_{\rm icfb}$. This in turn generates a current signal $I_{\rm icfb}$ that flows through both $\mathrm{M_{vtoi1}}$ and $\mathrm{M_{vtoi2}}$. $\mathrm{M_{vtoi3}}$ copies $I_{\rm icfb'}$ and generates $I_{\rm vtoi}$ [24], which flows through $\mathrm{M_{icfb1}}$ to create a voltage signal at the negative node of the error amplifier $\mathrm{EA_{icfb}}$.

By making $\mathrm{M_{vtoi1}}$ wide enough, we can obtain the transition voltage, $V_{\rm tr}$, from IC mode to CC mode using the following relationships:

$$V_{\rm tr} = R_{\rm voti} \times I_{\rm icfb(max)} = 5 - V_{\rm vtoi2} - V_{\rm vtoi1} \tag{8}$$

where 5 is the voltage supply, $V_{\rm vtoi1}$ is the overdrive voltage of $\mathrm{M_{vtoi1}}$, and $V_{\rm vtoi2}$ is the gate-source voltage of $\mathrm{M_{vtoi2}}$.

$V_{\rm vtoi1}$ and $V_{\rm vtoi2}$ can be expressed as

$$V_{\rm vtoi1} = \sqrt{\frac{2I_{\rm icfb(max)}}{K_n'\left(\frac{W}{L}\right)_{\rm vtoi1}}} \tag{9}$$

$$V_{\rm vtoi2} = V_{\rm thp} + \sqrt{\frac{2I_{\rm icfb(max)}}{K_p'\left(\frac{W}{L}\right)_{\rm vtoi2}}} \tag{10}$$

where $(W/L)_{\rm vtoi1}$ and $(W/L)_{\rm vtoi2}$ are the aspect ratios of $\mathrm{M_{vtoi1}}$ and $\mathrm{M_{vtoi2}}$, respectively. Hence,

$$V_{\rm tr} = 5 - \left[V_{\rm thp} + \sqrt{\frac{2I_{\rm icfb(max)}}{K_n'\left(\frac{W}{L}\right)_{\rm vtoi1}}} + \sqrt{\frac{2I_{\rm icfb(max)}}{K_p'\left(\frac{W}{L}\right)_{\rm vtoi2}}}\right] \tag{11}$$

By using some algebraic manipulation, we obtain

$$V_{\rm tr} = \sqrt{\frac{1}{\alpha^2} - 5 + V_{\rm thp}} - \frac{1}{\alpha} \tag{12}$$

where

$$\alpha = \frac{R_{\rm vtoi}}{2\sqrt{2}} \times \left[\sqrt{K_n'\left(\frac{W}{L}\right)_{\rm vtoi1}} + \sqrt{K_p'\left(\frac{W}{L}\right)_{\rm vtoi2}}\right]. \tag{13}$$

If $\mathrm{M_{vtoi1}}$ is narrow, $V_{\rm tr}$ will be limited by $5 - V_{\rm thn'}$. Note that due to body effect, $V_{\rm thn'}$ will be significantly larger than $V_{\rm thn}$. Hence, the mode transition voltage, $V_{\rm tr}$, can be defined as

$$V_{\rm tr} = min\left[\left(5 - V_{\rm thn'}\right), \left(\sqrt{\frac{1}{\alpha^2} - 5 + V_{\rm thp}} - \frac{1}{\alpha}\right)\right]. \tag{14}$$

Direct sensing of $I_{\rm Charge}$ to attain a precise current signal requires the addition of a current sensing resistor, which degrades efficiency significantly when the charging current is high. Instead, a replica circuit consisting of $\mathrm{M_{hvcs,rep}}$, $\mathrm{M_{ccc,rep}}$, $\mathrm{M_{Power,rep}}$, and $R_{\rm ics2}$ is used to generate $I_{Charge,rep}$, which is a fractionized $I_{\rm Charge}$. The gate of $\mathrm{M_{hvcs,rep}}$ is connected to the voltage supply, mimicking $V_{\rm cv}$ which is also pulled to the voltage supply by $\mathrm{EA_{cvfb}}$ before the charger enters CV mode. It is worth noting that the gate of $\mathrm{M_{hvcs,rep}}$ must be connected to the supply voltage internally, since N-type LDMOS transistors are susceptible to ESD [25]. The value of $R_{\rm ics2}$ should be

made close to $R_{\rm cvs}$, but direct matching between the two is unnecessary. The mismatch between the two resistance will only cause negligible effect on $I_{\rm Charge,rep}$ during IC mode.

$\rm EA_{icfb}$ indirectly drives $\rm M_{vcs,rep}$ through $\rm M_{icls1}$ and $\rm M_{icls2}$ to steal current $I_{\rm vcs,rep}$ from $I_{ccc,rep}$, which is the drain current of $\rm M_{ccc,rep}$. Consequently, $I_{\rm Charge,rep}$ flowing through $\rm M_{Power,rep}$ and $\rm M_{icfb2}$ is scaled proportionally to $I_{\rm ccc,rep}$. $\rm EA_{icfb}$ regulates the voltage generated by $I_{\rm Charge,rep}$ to the voltage generated by $I_{\rm vtoi}$, which simultaneously regulates the current $I_{\rm Charge,rep}$ itself to $I_{\rm vtoi}$. Since the gate of $\rm M_{vcs}$ and $\rm M_{vcs,rep}$ are driven by the same voltage, $V_{\rm icadj}$, the amount of current $I_{\rm vcs}$ stolen from $I_{\rm ccc}$ will be proportional to the amount $I_{\rm vcs,rep}$ stolen from $I_{\rm ccc,rep}$. Hence, $I_{\rm Charge}$ will be proportional to $I_{\rm Charge,rep}$, which in turn is proportional to the feedback voltage, $V_{\rm icfb}$.

Throughout the charging sequences, the IC loop and the CV loop do not interact with each other. Whenever a loop is controlling the behavior of the charger, the other loop is saturated such that it cannot affect the operation of the charger. Hence, stability issues are dramatically simplified and smooth transition between charge modes is ensured regardless of what mode the charger is.

D. Antenna Effect Protection Pad

The antenna effect, more formally known as the plasma induced gate oxide damage, can potentially damage integrated circuits during the manufacture process [27]–[31]. Such an effect occurs when the metal connected to the gate of a MOS transistor somehow acquires a voltage higher than the maximum sustainable voltage of that transistor during fabrication. Since the gate dielectric is only a few molecules thin, breakdown may occur [31]. Furthermore, if an input transistor of a differential pair is subject to the plasma induced gate oxide damage, an offset voltage is induced [32] and the overall system closed-loop accuracy is degraded. To prevent plasma induced gate oxide damage, foundries often provide antenna rules based on antenna ratio, AR, which is the allowable ratio of metal area to gate area. The definition of AR can be found in [33], [34]. However, since the ultra-thick top metal (UTM) thickness of this process is 30 kÅ (3 μm) [8], the height of both the metal and the polysilicon should be taken into account:

$$\rm AR = \frac{\kappa(W_M \times L_M \times H_M)}{W_P \times L_P \times H_P} \tag{15}$$

where W_M, L_M, H_M are the width, length, and height of the metal, respectively. W_P, L_M, and M_P are the width, length, and height of the polysilicon of the MOS transistor connected to the metal. κ is a coefficient.

A bonding PAD typically consumes an area of 70 μm$\times$80 μm on all three metal layers. Hence, transistors with their gate node connected to bonding pads must be large enough to meet the minimum AR requirements. Unfortunately, such requirements restrict the user from connecting an external node to small transistors such that unnecessary dilemmas regarding the selection of transistor aspect ratios may appear. To resolve this issue, the proposed antenna effect protection pads can be deployed instead of standard pads. The antenna effect protection PAD is obtained by adding a dummy 0.5 μm PMOS transistor beneath the standard PAD, as shown in Fig. 13. Notably, both drain and source of the PMOS transistors are coupled to Metal 1 (M1) using contacts. The drain and source node can provide forward diode connection when a voltage is higher than 5 V appears on any metal layers so that the gate oxide of the connected small transistors is protected. The isolation rings are connected to ground and the 5 V supply voltage, respectively. Since the N-well is also connected to the 5 V supply voltage and drain/source are shorted together, high dc impedance is achieved. Parasitic capacitance existing between bulk and the other three shorted terminals is at its minimum value, since the PMOS is in cut-off region. Hence, antenna effect protection pads have negligible impact on circuit behavior while providing adequate protection to meet the AR requirements set by foundries. The parasitic capacitance can be estimated as [35]

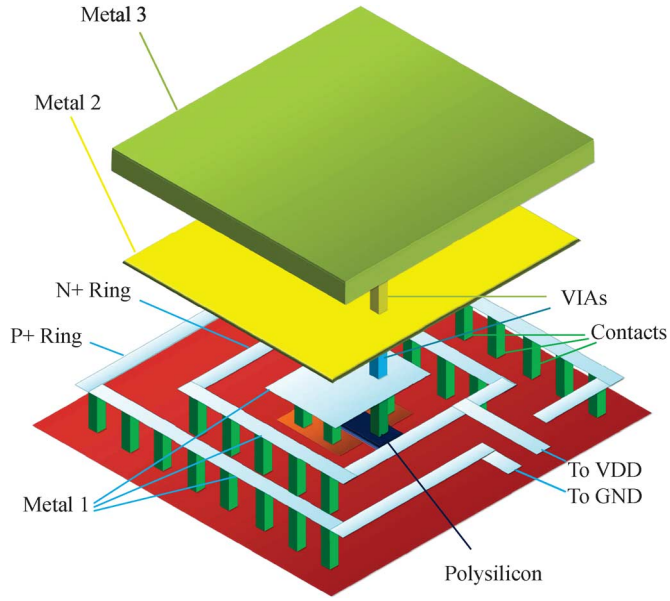

Fig. 13. The antenna effect protection PAD.

$$C_{\rm pad} \approx \varepsilon_{\rm ox}\left[1.15 \times \frac{A_{\rm pad}}{h} + 1.4 \times p_{\rm pad} \times \left(\frac{t}{h}\right)^{0.222}\right] \tag{16}$$

where $A_{\rm pad}, p_{\rm pad}$ and t are the area, periphery, and thickness of the antenna effect protection pad, respectively. h is the distance of the bottom metal plate to the substrate, and $\epsilon_{\rm ox}$ is the dielectric constant of SiO_2. Since the M1 layer is removed, h is increased and the total parasitic capacitance is reduced.

Finally, since antenna effect protection pads do not require additional silicon area, they can be placed without increasing the total layout cost of the chip.

V. Experimental Results

To evaluate the charging current with respect to the battery voltage, the targeted battery load of 14 $\times$ 4.2 V Li-ion batteries are emulated with Prodigi 3311D programmable dc electronic load, and the variable voltage is supplied by a Chroma 62012p-600-8 programmable power supply.

As shown in Fig. 14, the charger begins with a charging current of 36 mA, which slowly rises to 136 mA. To improve efficiency, resistor $R_{\rm cvs}$ is increased to 20 kΩ instead of the value

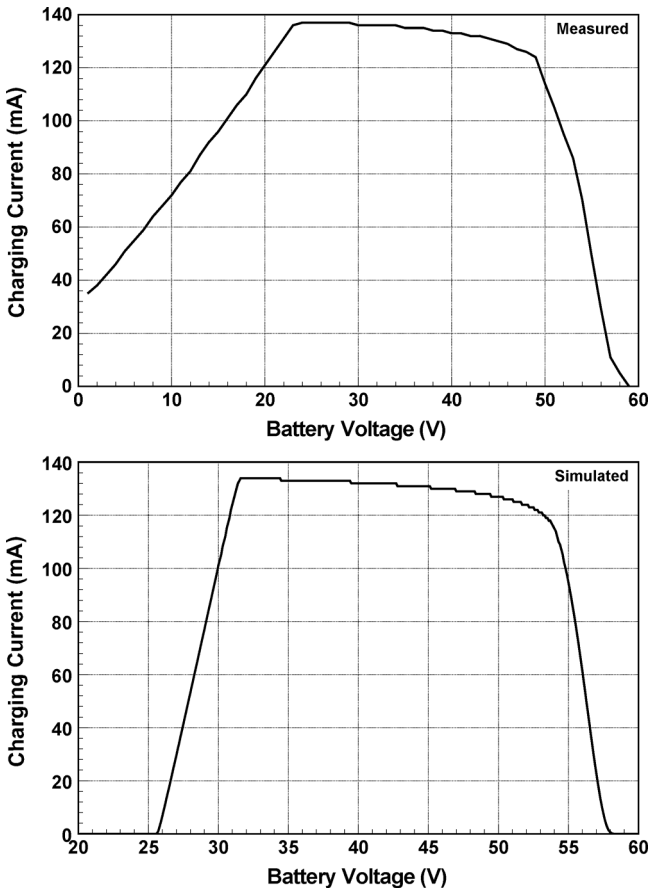

Fig. 14. Measured charging current and simulated charging current of the charger as a function of the battery voltage.

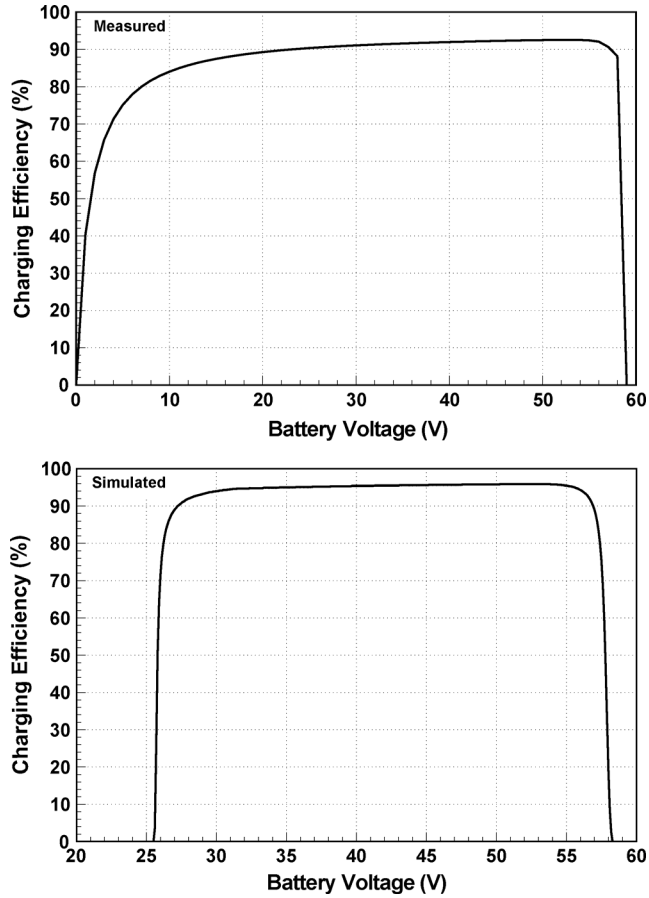

Fig. 15. Measured charging efficiency and simulated charging efficiency of the charger as a function of the battery voltage.

14.5 kΩ used in simulation. It has caused an impact on the characteristics of the charger in IC mode, but it is possible to remove the deviation if $R_{\rm ics2}$ is also connected externally and made equal to $R_{\rm cvs}$. These results are tolerable, since they only interfere with the initial charge sequence of the batteries. IC mode neither determines when the battery transits from CC mode to CV mode nor decides when the charge sequence ends. Charging efficiency with respect to the battery voltage is plotted in Fig. 15. This charger has a peak efficiency up to 92% during the charging sequence. Notably, even a deeply uncharged 4.2 V battery may still have more than 2 V such that a series of 14 batteries should at least have a voltage of 28 V. Therefore, the simulated low efficiency below 26 V shown in Fig. 15 would never occur in practical scenario.

The proposed chargers have been fabricated using TSMC 0.25 μm BCD 60 V technology. The chip shown in Fig. 16 was proposed in [12]. It features diode-based constant current clamp, which has a high sensitivity to process and temperature variation. The TC mode of this charger is unusable, since an inductive kickback it induces permanently damages the charger occurs when triggered. It occupies a total silicon area of $586 \times 879\ \mu{\rm m}^2$ (with pads).

The TC mode has been replaced with IC mode in the chip shown in Fig. 17. Unlike its earlier counterpart which used low voltage transistors with long lengths, feature-sized transistors were used instead. This greatly reduces silicon area occupied

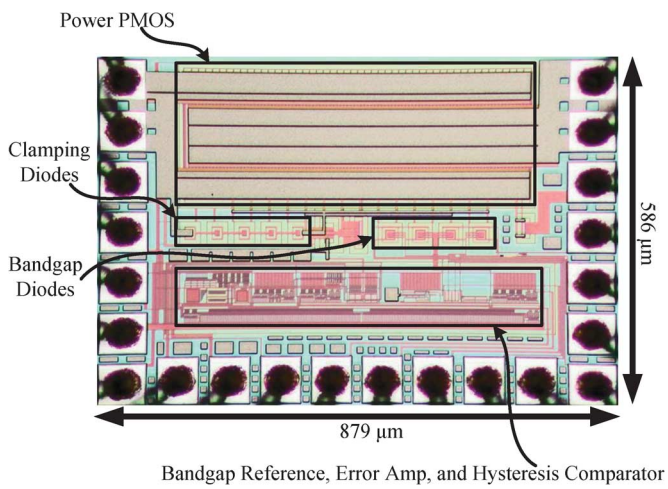

Fig. 16. The die photo of the charger with bandgap reference, hysteresis comparators, and diode-based constant current clamp.

by low voltage (LV) circuits. Since this charger is intended to be integrated into a complete BMS solution in the future, $V_{\rm cvref}$ is made to be adjustable so that bypassing batteries from the charging path can be achieved. Hence, the bandgap reference is removed so that $V_{\rm cvref}$ can be adjusted directly using a digital-to-analog converter (DAC). This charger occupies a total silicon area of $414 \times 900\ \mu{\rm m}^2$ (with pads).

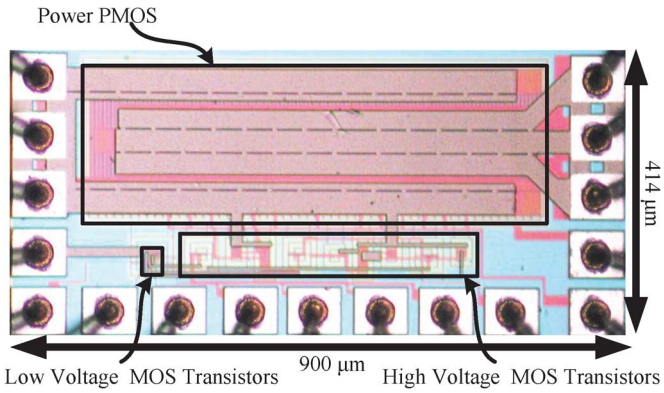

Fig. 17. The die photo of the charger supporting IC/CC/CV charge modes.

TABLE I
CHARGER COMPARISON

	[12]	This Work
Supply Voltage	60 V	60 V
Maximum Charge Current	52 mA	136 mA
Peak Efficiency	80 %	92 %
Supported Charge Modes	CC Mode CV Mode TC Mode (×)	CC Mode CV Mode IC Mode
Over Temperature Protection	Yes	No
Antenna Effect Protection	No	Yes
Silicon Area	586 × 879 μm^2	414 × 900 μm^2
Year	2011	2012

(×) Denotes not functional.

Finally, a comparison of these two chargers is tabulated in Table I. Since TC mode is not functional, it is denoted with a "×" symbol.

VI. CONCLUSION

A 60-V high voltage charger capable of charging 14 serially connected 4.2-V lithium-ion batteries with smooth charge mode transition is presented along with measured results. The circuit combines two different regulation loops into a single circuit with smooth transition between different modes. High efficiency is achieved by sourcing a variable voltage supply that tracks the voltage of the batteries to reduce unwanted power dissipation. This design is carried out using the TSMC 0.25 μm BCD 60-V technology.

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