On-Chip Process and Temperature Monitor for Self-Adjusting Slew Rate Control of 2 × VDD Output Buffers

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***Abstract*—A novel process and temperature compensation design for 2 × VDD output buffers is proposed, where the threshold voltages (Vth) of PMOSs and NMOSs varying with process and temperature deviation could be detected, respectively. A prototype 2 × VDD output buffer using the proposed compensation design is fabricated using a typical 0.18 μm CMOS process. By adjusting output currents, the slew rate of output signals could be compensated over 117%. The maximum data rate with compensation is 120 MHz in contrast with 95 MHz without compensation, which is measured on silicon with an equivalent probe capacitive load of 10 pF.**

***Index Terms*—Floating N-well circuit, gate-oxide reliability, mixed-voltage-tolerant, output buffer, process and temperature variation, threshold voltage detection.**

I. Introduction

THE sensitivity of modern VLSI circuits to process, and temperature (PT) variation degrades the performance and the yield, particularly when the technology is evolved toward nano-scale. The performance of VLSI circuits can be deemed as a function of PT variation, as shown in Fig. 1. If PT compensation is available, the acceptable envelope can be elevated to a larger area with high performance. Many approaches have been reported to resolve the PT variation detection [1]–[17].

A digital on-chip technique was proposed to detect local random variation of MOSFET current basing on the relationship between process variation and threshold voltage (Vth) [1], [2]. [3], [4] proposed the process control-monitor (PCM), consisting of 4 modules, i.e., racer, distributed jitter, leaker, and distributed ring oscillator, to detect across-die process variation. Another PCM method using a ring buffer and a pulse counter to detect process variability was revealed in [5], [6], which could monitor the process variations of PMOS and NMOS, respectively. Traditionally, temperature detectors are categorized into two different types, i.e., voltage detection and digital detection. The voltage detection scheme basically comprises a temperature sensor and an analog to digital converter (ADC). The temperature sensor at least possesses a temperature-sensitive feature or measure to generate a temperature-sensitive voltage. Then, the ADC converts the temperature-sensitive voltage into a digital code. Notably, the conversion between voltage and temperature is expected to be linear to attain high precision. Usually, the range of temperature-sensitive voltage is close to 100 mV from 0 °C to +100 °C such that a high precision ADC is required to distinguish the difference in such a small voltage window. Thus, a sigma-delta ADC is widely used in this kind of temperature detectors [7]. Notably, a high precision sigma-delta ADC is not easy to design in a fully digital circuit.

Recently, many researchers turn their attention to the digital detection scheme. There are two kinds of temperature sensors for this type, i.e., oscillator [8], and delay cells [9]. Referring to [8], the frequency of the oscillator shall be varied with the temperature. Depending on the sensitivity between temperature and the oscillator, a frequency to temperature converter (FTC) is used to convert the frequency into digital codes. The other way is to detect the temperature variation by the delay time of delay cells [9]. When the temperature is increased, the delay time of delay cells is increased, and vice versa. Therefore, delay cells

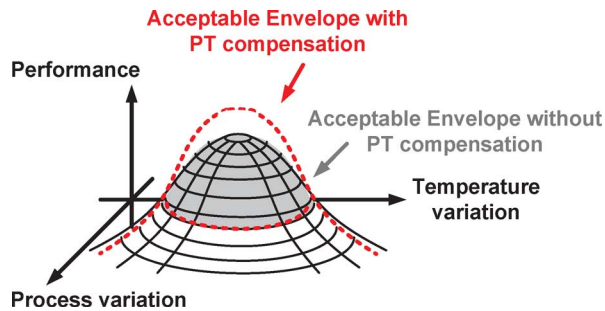

Fig. 1. Performance envelop as a function of process and temperature variation.

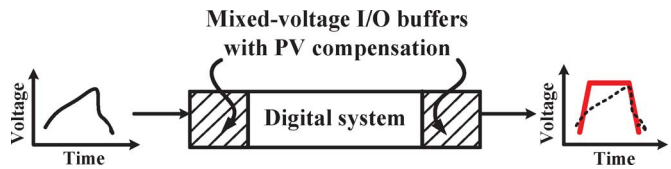

Fig. 2. The slew rate compensation scenario.

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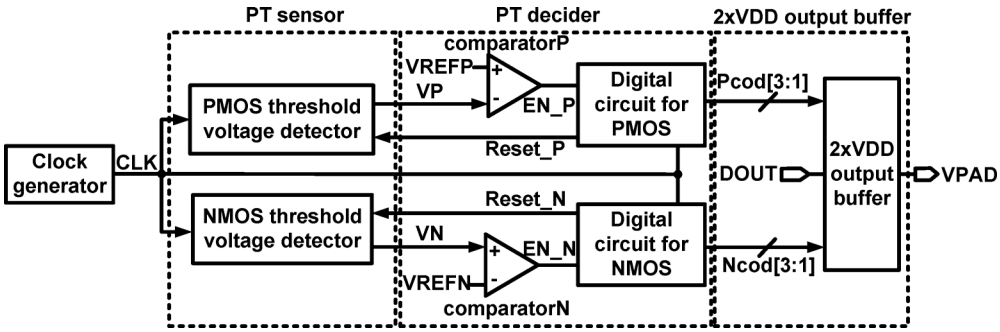

Fig. 3. The block diagram of the proposed system.

are as good as the oscillator in a temperature detector. The digital temperature detector is very welcomed in a system-on-chip (SoC) design. The reason is that the oscillator and delay cells are digital circuits, which are easily implemented and integrated by hardware description language, e.g., Verilog. Notably, the frequency of the oscillator may be drifted because of different processes, and the area is too large to be implemented in an I/O buffer. Though the delay-based method has also been applied to detect PVT variation [10]–[17], it can only recognize three corners, TT, FF, and SS. This kind of methods is proved to have problem to detect FS and SF process corners. The reason is that it is not able to examine the process variation of PMOS and NMOS, respectively.

Moreover, for the high-speed interface circuits, different slew rate is required by many communication systems, e.g., PCI and PCI-express. Hence, a compensation mechanism with NMOS and PMOS threshold voltage detectors is needed to self-adjust the slew rate of output buffers, as shown in Fig. 2.

The rest of this investigation is organized as follows. In Section II, the functions of process and temperature detectors are described in detail, respectively. In Section III, the proposed 2 × VDD output buffer is compensated by the outputs of process and temperature detectors. In Section IV, the measurement results, including die photo, measurement waveform, and measurement environment, are given to justify the function of the proposed design. The performance comparison between our output buffer and prior works is given as well. In Section V, a brief conclusion is given.

II. Process and Temperature Detection

Fig. 3 shows the block diagram of the proposed system comprising a clock generator, PT (process and temperature) sensor, PT decider, and a 2 × VDD output buffer. The clock generator is composed of multiple cascaded inverters to be a ring oscillator to generate the clock of PT sensor and PT decider. PT sensor consists of an NMOS threshold voltage detector and a PMOS threshold voltage detector, which generate two different voltages, VP and VN, respectively, to PT decider. PT decider is in charge of distinguishing the process and temperature variation of MOS, which is composed of two comparators, e.g., comparatorN and comparatorP, and Digital circuits for NMOS and PMOS.

A. NMOS Threshold Voltage Detector

Referring to Fig. 4, the NMOS threshold voltage detector schematic is shown. Fig. 5 illustrates the detection steps as follows.

Step_0: When $\mathrm{Reset\_N}$ is VDD and CLK is 0 V to activate the NMOS threshold voltage detector, net902 is discharged to 0 V. At the same time, net901 is charged to $(\mathrm{VDD} - \mathrm{Vthn}_{\mathrm{MN901}})$, where $\mathrm{Vthn}_{\mathrm{MN901}}$ is the threshold voltage of MN901. $(\mathrm{VDD} - \mathrm{Vthn}_{\mathrm{MN901}})$ equals to the voltage across the capacitor C90.

Step_1: $\mathrm{Reset\_N}$ is 0 V and CLK is pulled up to VDD, and then net902 is pulled down to $(\mathrm{Vth}_{\mathrm{MN901}} - \mathrm{VDD})$ due to the capacitor, C90. At the same time, MN906 is turned on to charge net902 to $(-\mathrm{Vth}_{\mathrm{MN901}})$. When CLK is dropped from VDD to 0 V again, net902 is pulled up to $(\mathrm{VDD} - \mathrm{Vth}_{\mathrm{MN901}} - \mathrm{Vth}_{\mathrm{MN906}})$. Hence, VN is charged to $(\mathrm{VDD} - \mathrm{Vth}_{\mathrm{MN901}} - \mathrm{Vth}_{\mathrm{MN906}} - \mathrm{Vth}_{\mathrm{MN907}})$ after the first charging cycle.

Step_2: When CLK is pulled up from 0 V to VDD again, net902 is pulled down to $(-\mathrm{Vthn})$ V. Simultaneously, MN904 is turned on by CLK such that net902 is charged to $(\mathrm{VDD} - \mathrm{Vth}_{\mathrm{MN901}} - \mathrm{Vth}_{\mathrm{MN906}} - \mathrm{Vth}_{\mathrm{MN907}} - \mathrm{Vth}_{\mathrm{MN903}})$ through MN903, MN904, and MN905. When CLK is dropped from VDD to 0 V again, net902 is pulled up to $(2\mathrm{VDD} - 2\mathrm{Vth}_{\mathrm{MN901}} - \mathrm{Vth}_{\mathrm{MN906}} - \mathrm{Vth}_{\mathrm{MN907}} - \mathrm{Vth}_{\mathrm{MN903}})$. Hence, VN is charged to $(2\mathrm{VDD} - 2\mathrm{Vth}_{\mathrm{MN901}} - \mathrm{Vth}_{\mathrm{MN906}} - 2\mathrm{Vth}_{\mathrm{MN907}} - \mathrm{Vth}_{\mathrm{MN903}})$ after the second charging cycle.

Step_N: After N charging cycles similar to the previous 1st and 2nd cycles, the voltage of VN is obviously derived as

$$\mathrm{VN}(N) = (\mathrm{VDD} - 3 \times \mathrm{Vthn}) \times N \tag{1}$$

where VDD is the supply voltage, Vthn is the threshold voltage of NMOS (assume all NMOS transistors have same threshold voltage), and N is the number of clock cycles.

Therefore, the voltage of VN will rise with the cycle count. However, the rising rate is determined by Vthn and VDD according to (1). The clock count needed for VN to reach the reference voltage level, VREFN, will then be different at different PT corners, as shown in Fig. 6. By differentiating the clock count, corner variations will be detected precisely. Notably, VN is then coupled to the plus input of comparatorN, as shown in Fig. 3.

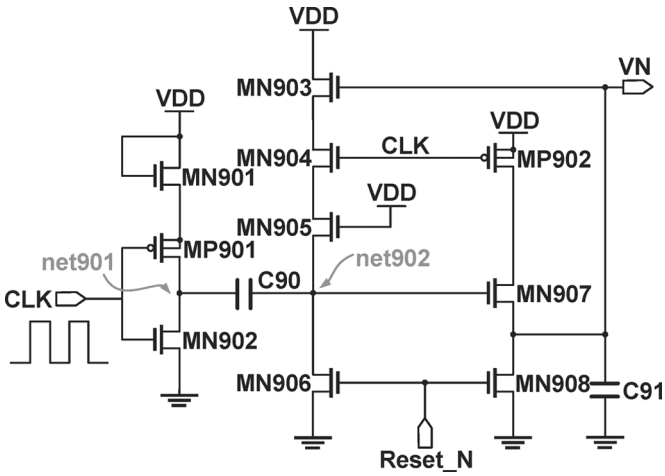

Fig. 4. NMOS threshold voltage detector.

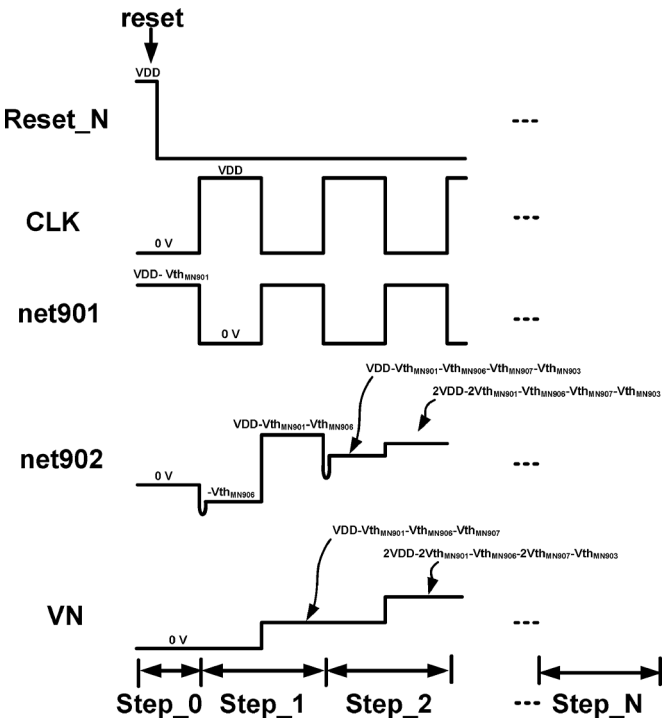

Fig. 5. The state transitions of the NMOS threshold voltage detector.

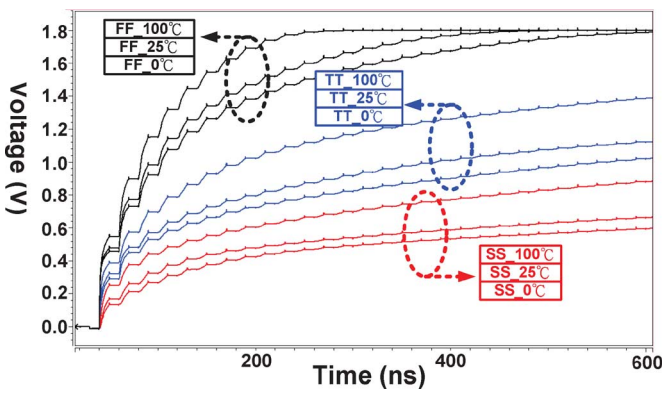

Fig. 6. Simulation waveform of NMOS threshold voltage detector.

B. PMOS Threshold Voltage Detector

The design concept of this detector is similar to that of the NMOS threshold voltage detector, as shown in Fig. 7.

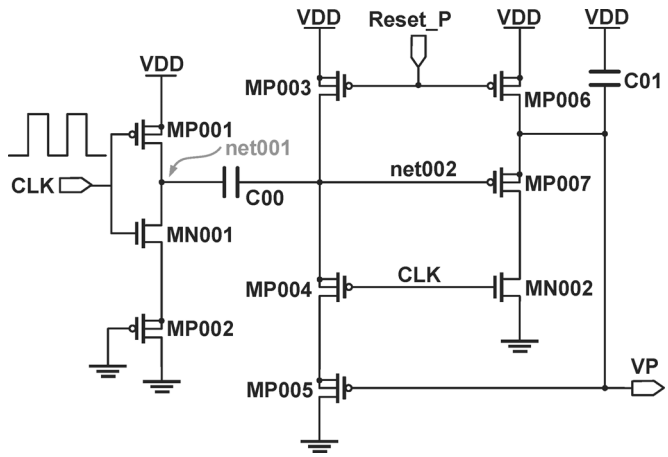

Fig. 7. PMOS threshold voltage detector.

Fig. 8 shows a total of M steps that are required for the PMOS threshold voltage detector as follows.

Step_0: When Reset_P is 0 V and CLK is VDD, net002 is charged to VDD through MP003. At the same time, net001 is discharged to $(\mathrm{Vth}_{\mathrm{MP002}})$, where $\mathrm{Vth}_{\mathrm{MP002}}$ is the threshold voltage of MP002. When CLK is 0 V, net001 is charged to VDD through MP001. The net002 is pulled up to $(2\mathrm{VDD}+\mathrm{Vth}_{\mathrm{MP002}})$ by C00, while MP003 is turned on to discharge net002 until $(\mathrm{VDD}+\mathrm{Vth}_{\mathrm{MP003}})$.

Step_1: When CLK is VDD, net001 is charged to $(\mathrm{Vth}_{\mathrm{MP002}})$ and net002 is discharged to $(\mathrm{Vth}_{\mathrm{MP002}}+\mathrm{Vth}_{\mathrm{MP003}})$. Notably, Vp is discharged to $(\mathrm{Vth}_{\mathrm{MP002}}+\mathrm{Vth}_{\mathrm{MP003}}+\mathrm{Vth}_{\mathrm{MP007}})$ through MP004 and MP005. When CLK is pulled down from VDD to 0 V, net001 is pulled up to VDD. At the same time, net002 is also pulled up to $(\mathrm{VDD}+\mathrm{Vth}_{\mathrm{MP003}})$, while net002 is discharged to $(\mathrm{Vth}_{\mathrm{MP002}}+\mathrm{Vth}_{\mathrm{MP003}}+\mathrm{Vth}_{\mathrm{MP007}}+\mathrm{Vth}_{\mathrm{MP005}})$ through MP004 and MP005.

Step_2: When CLK is transited from 0 V to VDD, net002 is changed to $(2\mathrm{Vth}_{\mathrm{MP002}}+\mathrm{Vth}_{\mathrm{MP003}}+\mathrm{Vth}_{\mathrm{MP007}}+\mathrm{Vth}_{\mathrm{MP005}}-\mathrm{VDD})$. Therefore, VP is discharged to $(2\mathrm{Vth}_{\mathrm{MP002}}+\mathrm{Vth}_{\mathrm{MP003}}+2\mathrm{Vth}_{\mathrm{MP007}}+\mathrm{Vth}_{\mathrm{MP005}}-\mathrm{VDD})$.

Step_M: After M charging cycles, the voltage of VP is attained as follows.

$$\mathrm{VP}(M) = 3M \times \mathrm{Vthp} - (M-1) \times \mathrm{VDD} \tag{2}$$

where VDD is the supply voltage, Vthp is the threshold voltage of PMOS (assume all PMOS transistors have same threshold voltage), and M is the number of clock cycles similar to N in (1).

The difference from the NMOS threshold voltage detector is that the voltage level of the output signal, VP, drops with the clock count. Besides, the falling rate is determined by the threshold of PMOS, Vthp, and VDD. By reading the clock count when VP meets the reference voltage VREP, different PT corners could also be detected separately, as shown in Fig. 9. Notably, VP is fed into the minus input of the comparatorN, as shown in Fig. 3.

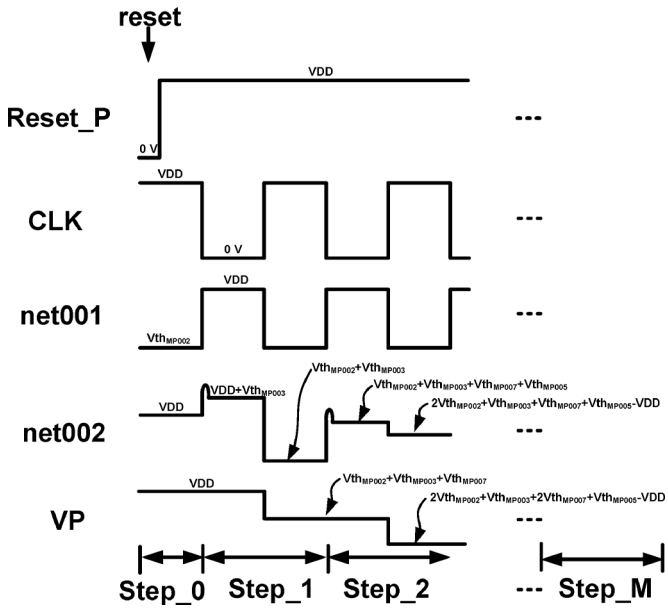

Fig. 8. The state transitions of the PMOS threshold voltage detector.

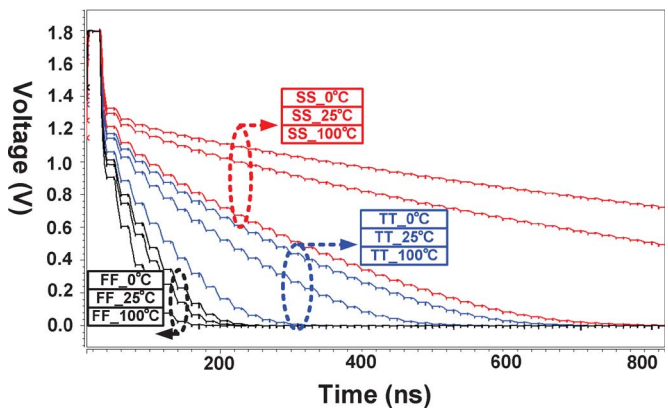

Fig. 9. Simulation waveform of PMOS threshold voltage detector.

C. Digital Circuits for NMOS and PMOS

Fig. 10 illustrates the block diagram of Digital circuits for NMOS and PMOS, respectively, where a 4-bit counter, an encoder, and D flip-flops are included in one Digital circuit. According to various corners, the encoder will generate a code to be latched in D flip-flops. When VP and VN reach the reference voltage VREFP and VREFN, respectively, comparators deliver, EN_P and EN_N, respectively, to latch D flip-flops. The code loaded into the D flip-flops, i.e., Ncode[3:1] and Pcode[3:1], indicates the required compensation status to compensate the output currents. Notably, Ncode[3:1] and Pcode[3:1] also can be used for more than one output buffers.

III. 2 × VDD Mixed-Voltage Tolerant Output Buffer With PT Compensation

The 2 × VDD mixed-voltage output buffer is composed of a Pre-driver, a Vg1 generator, a VDDIO detector, and an Output stage, as shown in Fig. 11. Pre-driver is used to encode three control signals, i.e., DOUT, Pcode[3:1], and Ncode[3:1], to adjust output currents for slew rate compensation. VDDIO detector and Vg1 generator can generate appropriate gate drive

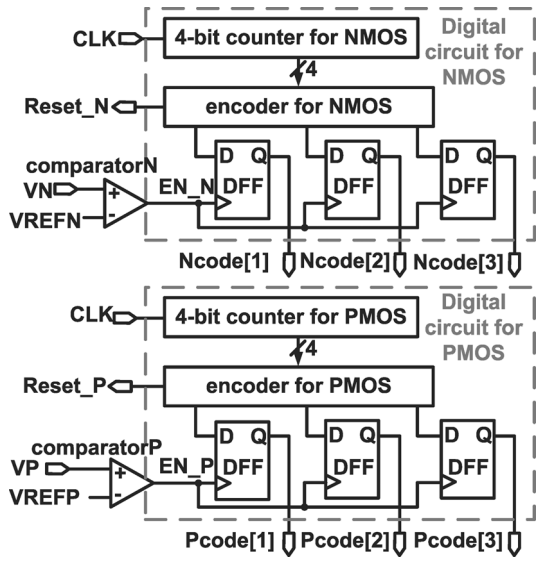

Fig. 10. Digital circuits for NMOS and PMOS.

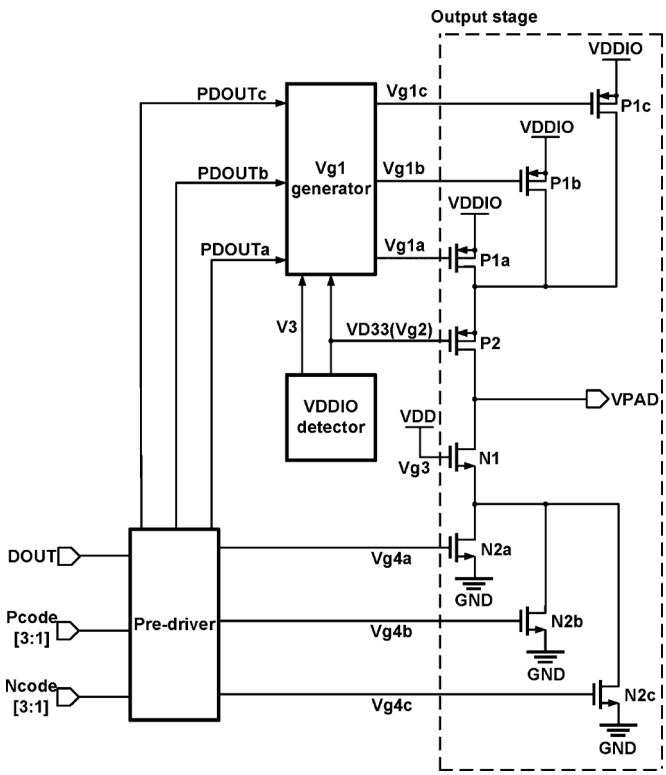

Fig. 11. 2 × VDD mixed-voltage tolerant output buffer.

voltages in different voltage modes without leakage currents and overstress problems [18]–[26].

A. Pre-Driver

The Pre-driver is a simple logic circuit to encode and predrive. After receiving and encoding three control signals, i.e., DOUT, Ncode[3:1], and Pcode[3:1], the driving current selection of the output stage will be determined. Take an example, the Pcode[3:1] and Ncode[3:1] to drive the Output stage, i.e., P1a–P1c and N2a–N2c. If the proposed I/O buffer is fabricated in slow corner, P1a–P1c and N2a–N2c all are turned on to drive

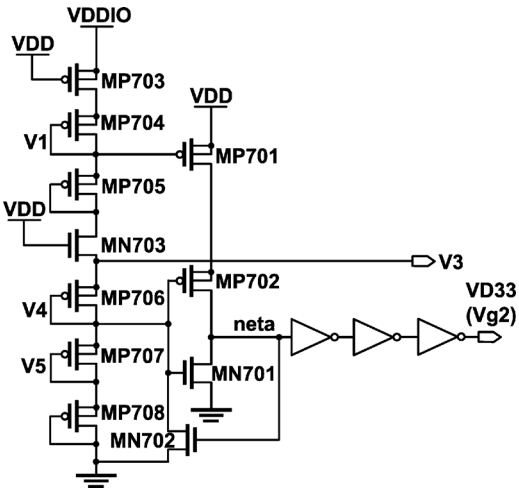

Fig. 12. VDDIO detector.

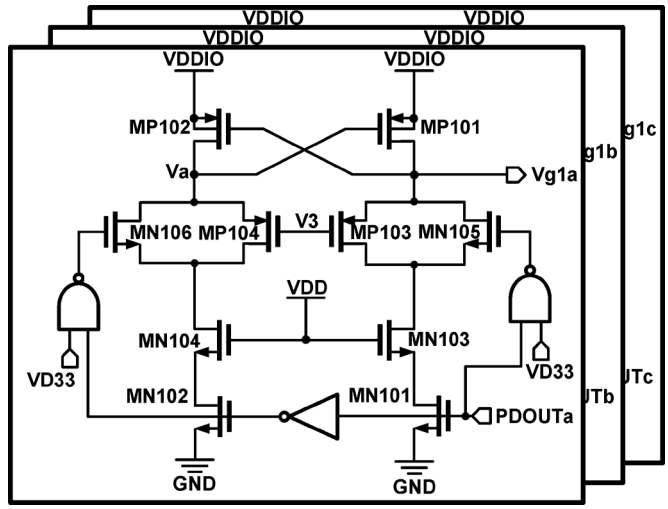

Fig. 13. Vg1 generator.

large current. By contrast, if the proposed I/O buffer is fabricated in fast corner, only P1a and N2a are turned on.

B. VDDIO Detector

As shown in Fig. 12, VDDIO detector is used to generate $\mathrm{VD33} = \mathrm{Vg2} = 1.8$ V to prevent the transistor P2 of Output stage from gate-oxide overstress problem when $\mathrm{VDDIO} = 3.3$ V. When $\mathrm{VDDIO} \leq 1.8$ V, VD33 is biased at 0 V to turn on the transistor P2. Meanwhile, VD33 is fed through into Vg1 generator to generate appropriate gate voltages for P1a–P1c of Output stage. The stacked diodes can generate different bias voltages, V1–V5, according to different VDDIOs. Therefore, by detecting the values of V1–V5, the voltage value of VDDIO can be determined. When $\mathrm{VDDIO} = 3.3$ V, MP703 is turned on to pull V1 up to 2.8 V to turn off MP701. At the same time, the transistor MP702 is added to keep the gate to source voltage of MP701 less than 1.8 V without overstress hazard. Then, when V4 is biased around 1 V to turn on MN701 and pull the voltage of neta down to 0 V, VD33 is output at logic 1. On the other hand, when $\mathrm{VDDIO} \leq 1.8$ V, MP703 is turned off and the voltage of neta is charged to 1.8 V. Then, MN702 is turned on to discharge V4 down to 0 V to turn off MN701 without leakage currents.

C. Vg1 Generator

Referring to Fig. 13, Vg1 generator in Fig. 11 is like a voltage level converter, which generates a pair of complementary signals, Vg1a, Vg1b, and Vg1c. Vg1 generator is composed of three same architectures of two cross-coupled PMOS transistors as a latch with stacked NMOS transistors in series as discharging paths. Take an example to generate Vg1a. In Tx mode, when VDDIO is 2 × VDD and the signal DOUT is logic 1, the voltage of PDOUTa (PDOUTb or PDOUTc) is logic 1 to turn on the MN101. Then, Vg1a can be discharged down to $\mathrm{V3} + \mathrm{Vthp}_{\mathrm{MP103}}$ through MP103, MN103, and MN101, where $\mathrm{Vthp}_{\mathrm{MP103}}$ is the threshold voltage of MP103. At the same time, MN102 is turned off to pull Va up to VDDIO, which can also turn off the MP101 to prevent any static leakage current path. By contrast, when the signal DOUT is logic 0, the voltage of PDOUTa (PDOUTb or PDOUTc) is logic 0 to turn off the MN101. Therefore, Vg1a can be charged up to VDDIO to turn off the P1a of Output stage.

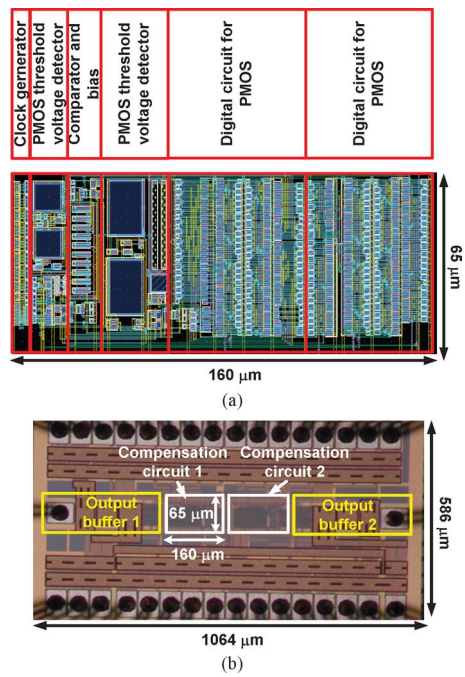

Fig. 14. (a) Layout of the compensation circuit. (b) Die photo of the proposed system.

D. Output Stage

Since the supply voltage (VDD) of the core circuits is 1.8 V using the 0.18 μm CMOS process, the output stage must be realized with two groups of stacked PMOS and NMOS transistors, respectively, for transmitting 2 × VDD signals, as depicted in Fig. 11 [20]–[25]. PMOSs P1a–P1c are connected in parallel so that the slew rate of the output signal can be compensated by adjusting the currents flowing through P1a–P1c. According to different PT scenarios, the control signal, Pcode[3:1] and Ncode[3:1], will select the number of turned-on PMOSs of the output stage. The selection of N1a–N1c is the same as

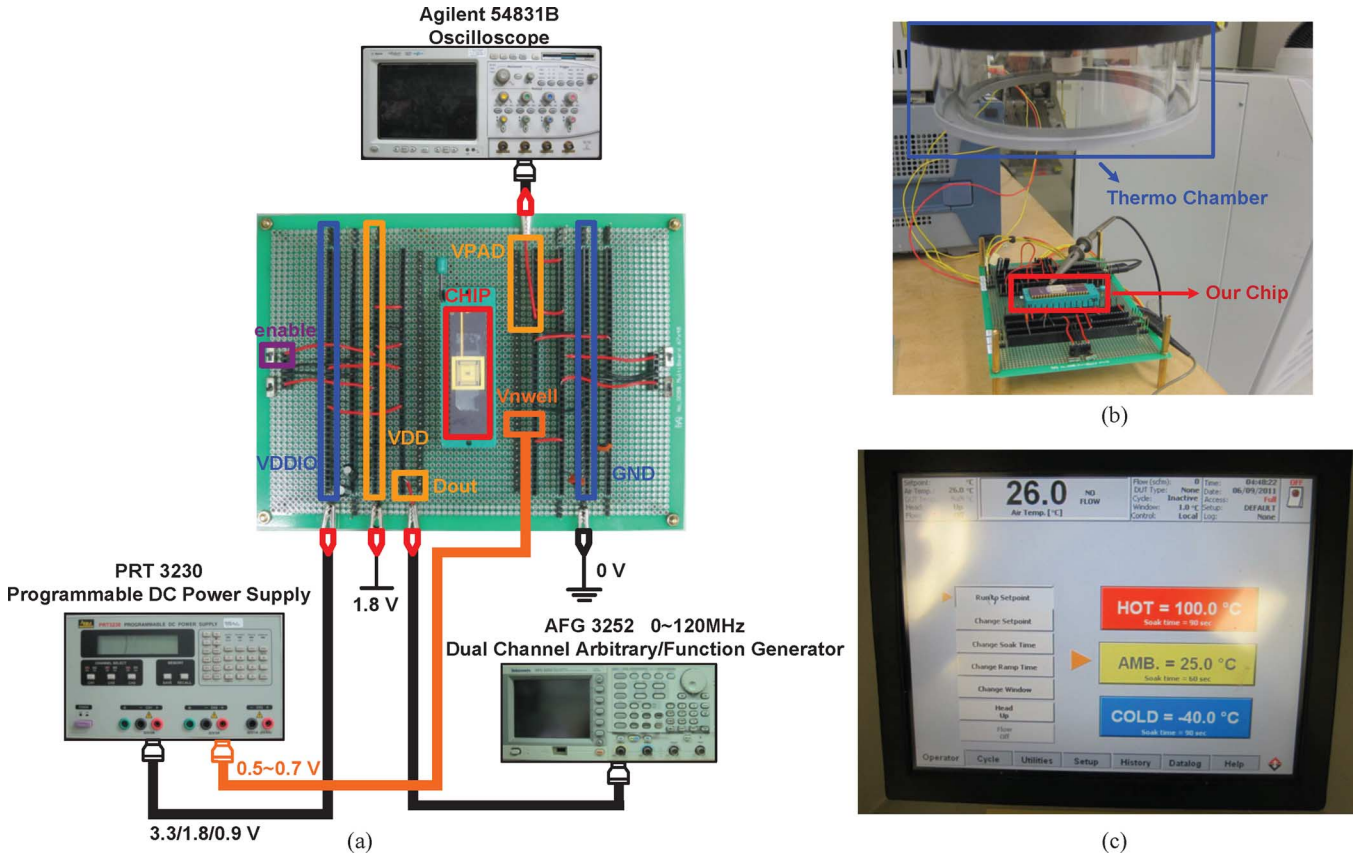

Fig. 15. The measurement settings of the proposed system. (a) In different transmitting modes when VDDIO is at 3.3/1.8/0.9 V. (b) The chip is heated and cooled down by a thermo chamber. (c) Thermo test is between −40 °C–100 °C.

PMOSs mentioned in the above. P1a–P1c and N1a–N1c are designed with different sizes to generate different currents, which could successfully achieve coarse and fine adjustment.

IV. Measurement Results

This work is fabricated using TSMC 0.18 μm CMOS technology without thick-oxide devices. Fig. 14 shows the layout and the die photo of the proposed design, where the 2 × VDD output buffer size is 329 μm × 65 μm and the compensation circuit area is only 160 μm × 65 μm.

Fig. 15 shows the measurement settings for PT compensation. Referring to Fig. 15(a), the body voltage of PMOSs, Vnewll, are varied from 0.5–0.7 V to emulate different process corners. Besides, VDDIO are supplied with 3.3/1.8/0.9 V, respectively, in different transmitting modes while VDD remains at 1.8 V. Fig. 15(b), (c) show that our chip is heated by a thermo chamber between −40 °C–100 °C.

Referring to Fig. 16–18, the maximum data rate of VPADs without compensation are measured to be 85/95/75 MHz when VDDIO is at 3.3/1.8/0.9 V given core VDD = 1.8 V, respectively. The worst improvement case of slew rate compensation, from 1.28 V/ns to 2.79 V/ns, occurs at [TT, 25 °C] corner when VDDIO = 3.3 V, as shown in Fig. 19. The maximum data rate is measured to 120 MHz with compensation. The performance comparison with several prior works is tabulated in Table I. Because our proposed design detects process variation independently for PMOS and NMOS, our proposed design is useful for

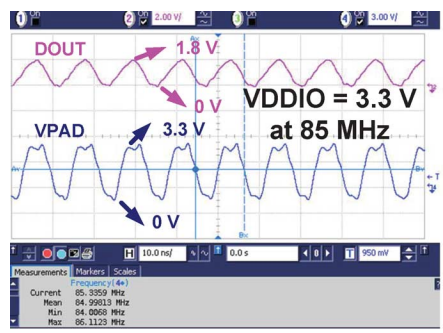

Fig. 16. The maximum data rate of VPAD when VDDIO is at 3.3 V.

all process corners, including FS and SF corners, compared with prior works. The area of our proposed design is 0.0104 mm^2. Equation (3) is used to normalize the area among different processes, as shown in Table II. After normalization, the normalized area of our design is 0.321, which is the second smallest area compared with prior works. Notably, the compensation circuit can be shared in many output buffers such that the area cost will not a serious overhead.

$$\text{Normalized area} = \frac{\text{Area}}{\text{Process}^2} \tag{3}$$

Therefore, our design has the edge of maximum slew rate improvement in measurement, the lowest power dissipation, and the capability to detect all process corners.

TABLE I
PERFORMANCE COMPARISON BETWEEN OUR DESIGN AND PRIOR WORKS

	Ours	[10] *TCAS-II*	[14] *JSSC*	[11] *TCAS-II*	[12] *ISCAS*
Year	2011	2010	2003	2007	2011
Process (μm)	0.18	0.18	0.18	0.13	0.065
Results	Measured	Measured	Measured	Measured	Measured
Slew rate (V/ns)	1.28-2.79	2.10-3.58	0.40-0.99	0.24	1.77
Process corners detected	TT, FF, SS FS, SF	TT, FF, SS	TT, FF, SS	TT, FF, SS	N/A
Area (mm^2)	0.0104	0.009	0.02807	0.063	0.0027
Power (mW)	0.427	13.7	N/A	N/A	0.5
Slew rate improvement	>117% (Measured)	>28% (Post-sim)	>32% (Measured)	>66% (Measured)	>143% (Post-sim)

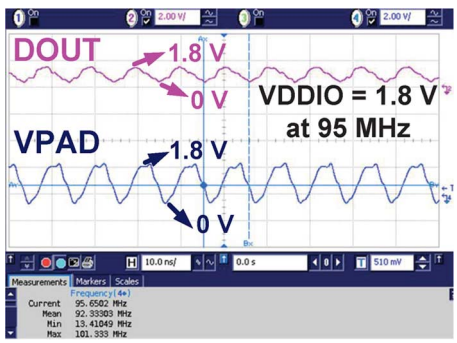

Fig. 17. The maximum data rate of VPAD when VDDIO is at 1.8 V.

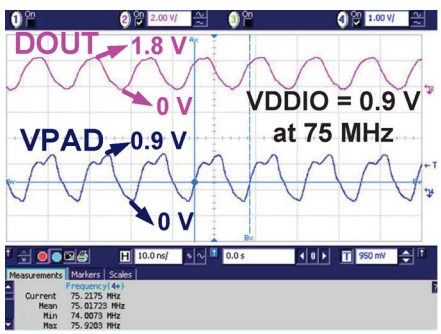

Fig. 18. The maximum data rate of VPAD when VDDIO is at 0.9 V.

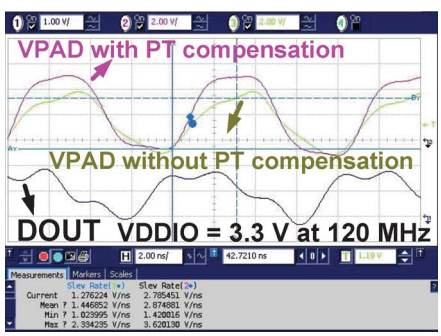

Fig. 19. When VDDIO $= 3.3$ V @120 MHz, the slew rate of VPAD can be compensated over 117%.

TABLE II
AREA COMPARISON BETWEEN OUR DESIGN AND PRIOR WORKS

	Ours	[10]	[14]	[11]	[12]
Area (mm^2)	0.0104	0.009	0.02807	0.063	0.0027
Normalized area	0.321	0.278	0.866	3.728	0.639

V. CONCLUSION

An on-chip process and temperature compensation and self-adjusting slew rate control technique for output buffers is proposed in this paper. The area of the compensation circuit is only 160 μm × 65 μm. Such an area overhead is affordable in any advanced process provided that one compensation circuit is shared by many buffers. Most important of all, the slew rate improvement can be achieved over 117% in addition to avoiding the gate-oxide overstress and the leakage current.

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