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A FlexRay Transceiver Design with Bus Guardian for In-car Networking Systems Compliant with FlexRay Standard

Chua-Chin Wang · Chih-Lin Chen · Gang-Neng Sung · Ching-Lin Wang · Chun-Ying Juan

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Abstract This paper presents a FlexRay Transceiver (FRT) with Bus Guardian (BG) used in an in-vehicle network compliance with FlexRay physical layer standards. FlexRay is a new standard for data/signal communication among electronic devices installed in a vehicle. The FRT includes two major parts in the physical layer design: the data transmission part, i.e., Bus Driver (BD), which is used to generate and recognize the electrical characteristics on the bus; the control part, including Bus Driver Controller and Bus Guardian (BG), which is in charge of data path, security, safety, and supervising Communication Controller (CC) in FlexRay communication systems. The proposed FRT with BG design in this work is implemented using a typical 0.18 μm CMOS process. The total core area is 0.88×0.84 mm^2 and the power consumption is 53.04 mW at a 80 MHz system clock by physical on-silicon measurement.

C.-C. Wang (✉) · C.-L. Chen · C.-L. Wang
Department of Electrical Engineering, National Sun Yat-Sen University, Kaohsiung, 80424, Taiwan
e-mail: ccwang@ee.nsysu.edu.tw

C.-L. Chen
e-mail: clchen@vlsi.ee.nsysu.edu.tw

G.-N. Sung
Design Service Department National Chip Implementation Center National Applied Research Laboratories, Taiwan 30078, Republic of China
e-mail: gnsung@cic.narl.org.tw

C.-Y. Juan
Metal Industries Research & Development Centre (MIRDC), Taipei 106, Taiwan
e-mail: chunying@mail.mirdc.org.tw

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1 Introduction

Car electronics have been widely recognized as the 4th "C" next to Computer, Communication and Consumer electronics [1, 2]. The car electronics cover power train, chassis safety, peripheral electronics control system, telematics communication system, in-vehicle networking, etc. For the sake of safety, entertainment, and comfortness in a vehicle, the speed and quality of data communication among ECUs (electronic control unit) must be enhanced. Therefore, an advanced control in-vehicle networking protocol seem to be needed to supervise all the automobile electronics, and synchronize existing networks. Prior in-vehicle networks were mainly composed of CAN (controller area network) or LIN (Local Interconnect Network) which emphasized safety and reliability. However, their limited 1 Mbps bandwidth is not sufficient for rapid growth of the data/signal transmission. By contrast, the MOST (Media Oriented Systems Transport) [3] network provided a very efficient mechanism for transporting massive media information, but lack of control capability.

FlexRay V2.1 is the latest in-car communication protocol [4] proposed by several automobile power houses, including BMW, Daimler-Chrysler, General Motors, Freescale, Philips, Bosch, Volkswagen, etc., in 2005. It was designed for data exchange among ECUs installed in a vehicle. FlexRay requires 10 Mbps data rate in either one of the two channels of an ECU for redundancy. If a single channel is used alone, the speed of the total data rate is expected to be 20 Mbps. Therefore, even the video signals, multimedia and control signals can communicate via the FlexRay

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Table 1 Comparison between FlexRay and CAN system.

	CAN	FlexRay
Bit rate	1 Mbps	10 Mbps
Channel	1 channel	2/1 channel (optional)
Network topology	Bus type	Mixed of bus and star types
Communication	Event triggered	Time + Event triggered
Oscillator	Ceramic/Crystal	Crystal oscillator
Network management	Software	Hardware
Network synchronization	Sync segment	Rate compensation

network with such a high data rate. The ultimate goal of the FlexRay protocol is that the automobile is X-by-wire (X = steer, break, accelerate, A/V, safety, etc..). Although FlexRay tends to resolve data communication challenges, FlexRay will not replace existing networks. By contrast, it can integrate and co-exist with existing network systems, including prior CAN, LIN, MOST and J1850 protocol, etc. In the next-generation vehicles, the FlexRay network is expected to be used in high-end applications, such as control and security, CAN networks will be focused on power train communication, and LIN networks are mainly for low-cost body electronics. Table 1 shows the comparison between FlexRay and the prior CAN-based systems.

Recently, many researches or products regarding the transceiver design used in FlexRay-based communication systems have been publicized. For example, FlexRay transceiver was implemented using a high-voltage process in [7–9]. However, they are high power consumption and not easily to be integrated with digital signal processors, which is usually implemented using a low-voltage process. FlexRay transceiver was then implemented using a typical 0.18 μm mixed signal CMOS process to attain 40 Mbps in a -40 °C $\sim$ $+125$ °C testing site in [10–12], which only verified the function of Bus Driver (BD) without Bus Guardian (BG), Bus Driver Controller, or a temperature detector. Besides, one of them was only proved by the simulation results rather than measurement results [12]. FlexRay communication networks with Active Star was physically implemented using ALTERA Excalibur ARM EPXA4F672C3 in [13]. This work only verified the functions by Verilog HDL language and ALTERA Excalibur ARM EPXA4F672C3, which is hard to justify reliability and safety in physical FlexRay systems.

In this paper, we propose a FlexRay Transceiver (FRT) design with Bus Guardian. In Section 2, we introduce the ECU node in a FlexRay system. A robust FRT is proposed, including Temperature Detector and Bus Driver (BD). In Section 3, we implement a Bus Guardian (BG) to fully conform to the FlexRay Standard V2.1. Finally, we compare the measurement results with FlexRay V2.1 and prior works in Section 4. A short conclusion is given in Section 5.

2 FlexRay Transceiver (FRT) Design

Figure 1 shows the explosive view of an ECU composed of Host, Communication Controllers (CC), and FRTs, where CC supervises the signals from BG and generates an error interrupt to Host if the scheduling of BG is misaligned. FRTs are used to transmit and receive data into/form the bus. Each ECU node transmits or receives data over two channels, i.e., Channel 1 and Channel 2. Figure 2 shows the proposed FRT design in this work, including a Bus Driver (BD), a Bus Driver Controller, a Power Manager, a

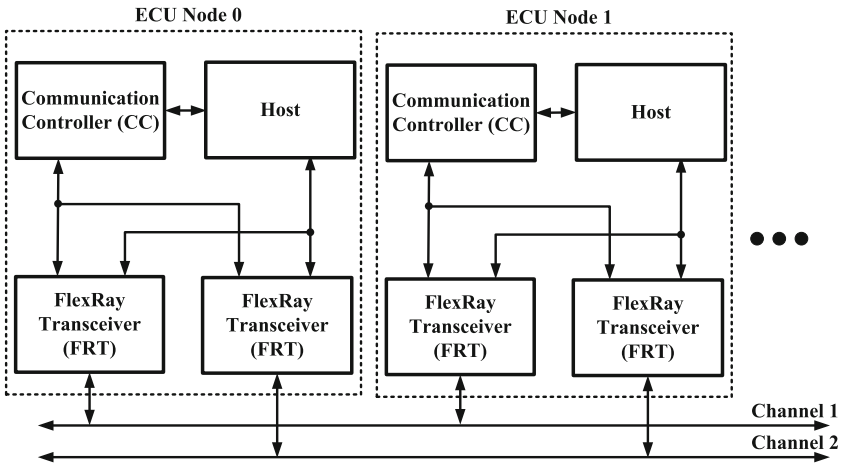


Figure 1 ECU nodes on the FlexRay bus.

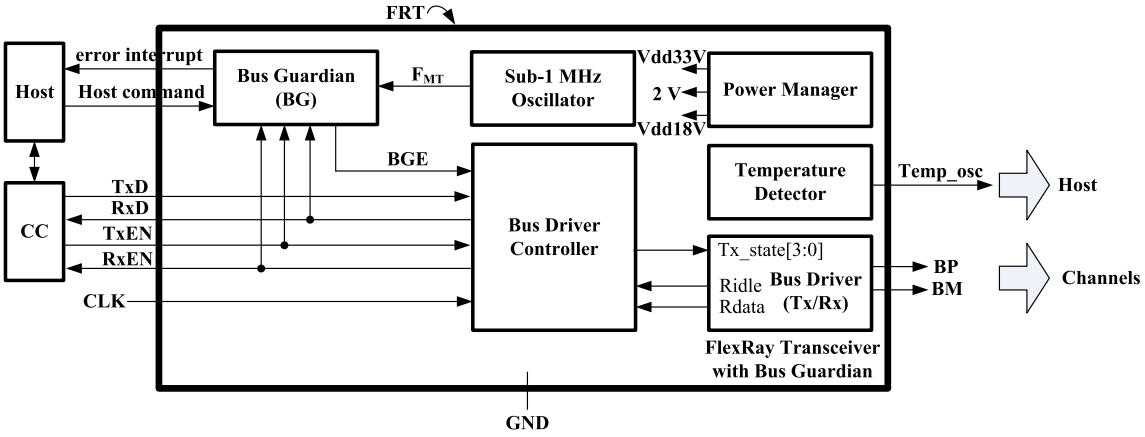


Figure 2 Explosive view of FlexRay Transceiver (FRT).

Temperature Detector, a Sub-1 MHz Oscillator, and a Bus Guardian (BG). Notably, a total of 2 sub-blocks are included in BD, which are Transmitter (Tx) and Receiver (Rx).

According to the FlexRay physical layer standards, a pair of signals, denoted as BP (Bus Plus) and BM (Bus Minus), are carried over one channel. BP and BM in fact are a pair of differential signals which can reduce the coupled noise on the bus by rejecting common-mode interference and ground offsets. The timing and amplitude characteristics of BP and BM required by the FlexRay standards are shown in Fig. 3.

The Tx was realized by an LVDS-like transmitter design [10] for transmitting data on bus, as shown in Fig. 4. According to state of Tx_state[3:0], which is an One-Hot code, the Tx control signals (Data0_C, Data1_C, Idle_C, and Idle_LP_C) are generated. Notably, Tx transmits differential signals on the bus that described in Table 2.

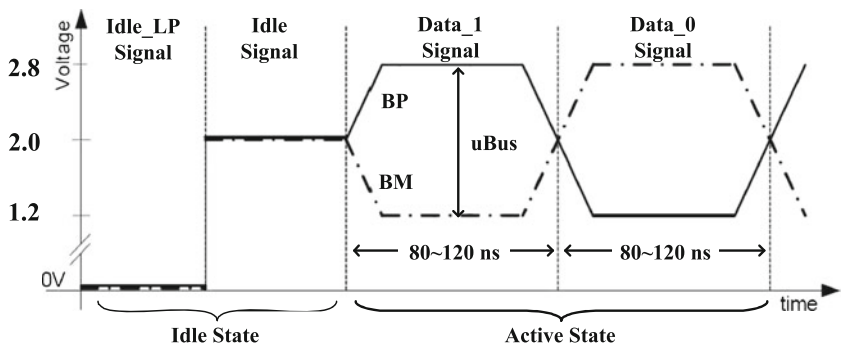
Apart from receiver circuits' design of traditional buses, Rx for FlexRay systems must recognize the Idle State besides slicing the received bits. Therefore, Rx was carried out by a 3-comparator scheme with hysteresis [10] for recovering the data from the bus, as shown in Fig. 5. Rx monitors the bus signal to generate Rdata and Ridle. If the bus is Idle or Idle_LP signal, Ridle is pulled high to logic '1'. If the bus is Data_1 signal, Rdata is pulled high to logic '1'. By contrast, if the bus is Data_0 signal, Rdata is pulled down to logic '0'.

Bus Driver Controller is used to command the state of Tx depending on the signal of TxEN (Tx enable), TxD (Tx data), BGE (BG enable), and Tx control signals as shown in Table 2. Bus Driver Controller receives the data from Rx through Rdata and Ridle. After Rdata and Ridle are activated over a predefined time length, Bus Driver Controller transfers the Rdata and Ridle to RxEN (Rx enable) and RxD (Rx data) to notify CC as described in Table 3.

Power Manager has been proposed in prior work [10], which generates Vdd18V and Vdd33V as 1.8 V and 3.3V supply voltage to all other sub-circuits in Fig. 2.

According to FlexRay specifications, a FlexRay system must be operated in $-40\ ^{\circ}\text{C} \sim +125\ ^{\circ}\text{C}$, which means a Temperature Detector, as shown in Fig. 2, is required to ensure that no hazards would be caused by temperature problems. Temperature Detector shall provide a means to monitor the junction temperature on silicon. If a predefined threshold is exceeded, Temperature Detector must

Figure 3 The required characteristics of BP and BM.



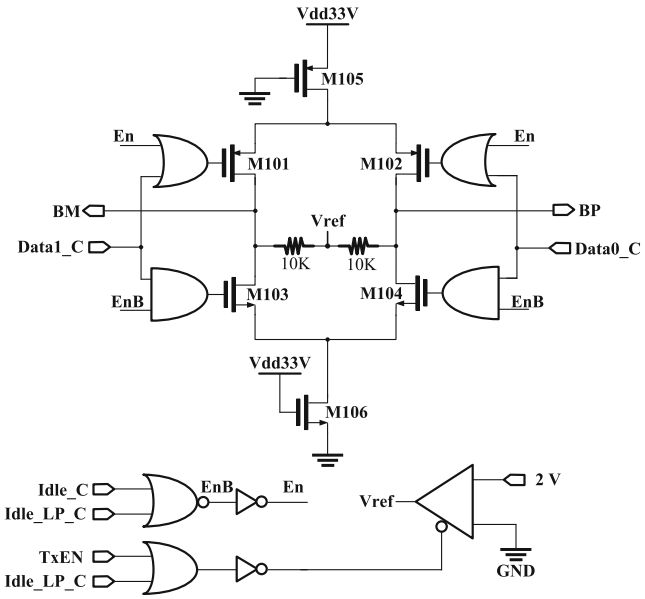


Figure 4 The schematic of Tx.

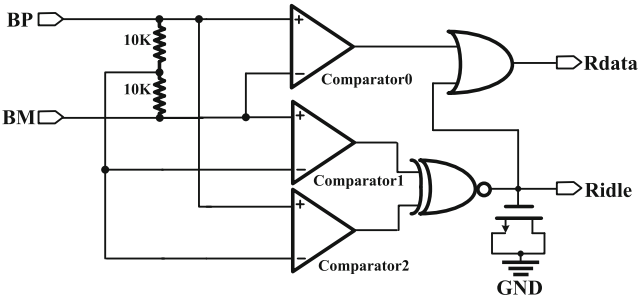


Figure 5 The schematic of Rx.

disable the transmitter, which usually demands the largest power consumption in a FlexRay system, to prevent further heating of the chip. Therefore, Temperature Detector plays an important role in a FlexRay system. Figure 6 shows the schematic of Temperature Detector, consisting of a ring oscillator, namely M02 $\sim$ M11, dummy cells, which are M12 $\sim$ M21, and a temperature-sensitive bias composed of Q01, Q02, R01, and M01. Referring to the temperature-sensitive oscillator in [14], the dummy cells are added to compensate the delay of each ring cell such that the duty cycle of Temp_osc will be very close to 50 %. BJT (Q01 and Q02) has a negative temperature coefficient. Q01 and Q02 are used to drive the gate of M01. Therefore, the operating current of M02 $\sim$ M11 are sensitive to temperature that is proved by following equations.

Referring to Eq. 1, Vs is 2 times of V_{BE}, which is the voltage difference between base and emitter of BJT. Equation 2 shows the temperature coefficient of V_{BE}, which is complementary to absolute temperature (CTAT). In Eqs. 3 and 4, R_{M02} and R_{M03} are the equivalent resistance between drain and source of M02 and M03, where β_{M02} is the beta value of M02 and Vth_{M02} is the threshold voltage of M02. β_{M03} and Vth_{M03} are defined similarly for M03. Equation 5 denotes Cg_{M04}, the total capacitance of M04 at gate. Cg_{M05}, Cg_{M14}, and Cg_{M15} are defined similarly for M05, M14, and M15, respectively. Notably, the frequency of Temp_osc is anti-proportional to the equivalent resistance and capacitance of every single stage, as shown in Eq. 6. The equivalent resistance and capacitance of the first stage, as shown in Fig. 6, are respectively shown in Eqs. 3–5. Substituting Eqs. 3–5 in Eq. 6 gives Eq. 7. According to Eqs. 7 and 8, '$\beta_{M02}(2 \times V_{BE} - Vth_{M02}) + \beta_{M03}(2 \times V_{BE} - Vth_{M03})$' becomes CTAT such that the frequency of Temp_osc is CTAT as well.

$$Vs = 2 \times V_{BE} \tag{1}$$

$$\frac{\partial V_{BE}}{\partial T} = -1.5\,\mathrm{mV/^oC} \tag{2}$$

$$R_{M02} = \frac{1}{\beta_{M02}(2 \times V_{BE} - Vth_{M02})} \tag{3}$$

$$R_{M03} = \frac{1}{\beta_{M03}(2 \times V_{BE} - Vth_{M03})} \tag{4}$$

$$Cg_{total} = Cg_{M04}||Cg_{M05}||Cg_{M14}||Cg_{M15} \tag{5}$$

$$\text{The frequency of Temp\_osc} \propto \frac{1}{(R_{M02}||R_{M03}) \times Cg_{total}} \tag{6}$$

Table 2 Bus state, BGE signal, and Tx_state protocol.

TxEN	TxD	BGE	Tx_state	Data0_C	Data1_C	Idle_C	Idle_LP_C	bus state
1	X	X	0010	0	0	1	0	Idle
X	X	0	0010	0	0	1	0	Idle
0	0	1	0100	1	0	0	0	Data_0
0	1	1	1000	0	1	0	0	Data_1
X	X	X	0001	0	0	0	1	Idle_LP

X=don't care

Table 3 Bus state and Rx protocol.

bus state	Rdata	Ridle	RxD	RxEN
Idle_LP	1	1	1	1
Idle	1	1	1	1
Data_0	0	0	0	0
Data_1	1	0	1	0

The frequency of Temp_osc $\propto$

$$\frac{\beta_{M02}(2 \times V_{BE} - Vth_{M02}) + \beta_{M03}(2 \times V_{BE} - Vth_{M03})}{Cg_{total}} \tag{7}$$

$$\frac{\partial \mathrm{Vth}}{\partial \mathrm{T}} = -1\,\mathrm{mV/^oC} \tag{8}$$

Notably, Sub-1 MHz Oscillator is a ring oscillator similar to the ring oscillator in Fig. 6 to generate a sub-1 MHz clock, which is F_{MT} signal, to drive BG. The details of BG and F_{MT} will be described in Section 3.

3 Bus Guardian Design

Bus Guardian (BG) is primarily used to receive commands from the Host, supervise the Communication Controller (CC), and receive frames on both channels. Depending upon the state of a BGE (BG enable) signal, BG enables the transmission of BD. Additionally, BG supervises TxEN signal from CC. In case of a misaligned slot scheduling of the CC, BG generates an error interrupt to Host.

Figure 7 shows an example of a communication cycle in a FlexRay system. A communication cycle includes four segments, i.e., Static Segment, Dynamic Segment, Symbol Window (SW), and Network Idle Time (NIT). Because only Static Segment and Dynamic Segment are allowed to convey data, BG arranges their priority according to an initial configuration. In Static Segment, each transmission frame length is fixed and counted by the number of "Slot". Every Slot of each node has been assigned in Static Segment, which is called time-triggered communication method to ensure data transmission on schedule. In Dynamic Segment, each transmission frame length is configurable for different applications. Each node or channel attains their bandwidths basing on their priority, namely event-triggered communication method. In other words, a higher priority node has a larger bandwidth for transmission. Notably, data with an unknown frame length is assigned in Dynamic Segment.

Referring to latest FlexRay Bus Guardian specification [23], we propose a BG architecture and interface shown in Fig. 8.

- Communication Controller (CC) also supervises the BGE signal from BG and generates an error interrupt to the Host, if the slot scheduling of BG is misaligned.
- BG consists of several function blocks, including Communication Controller Supervision (CCS), TxENSUP, NHC, NTALC, BGEGEN, CHC, and STARTUPSUP which will be given in the following text.

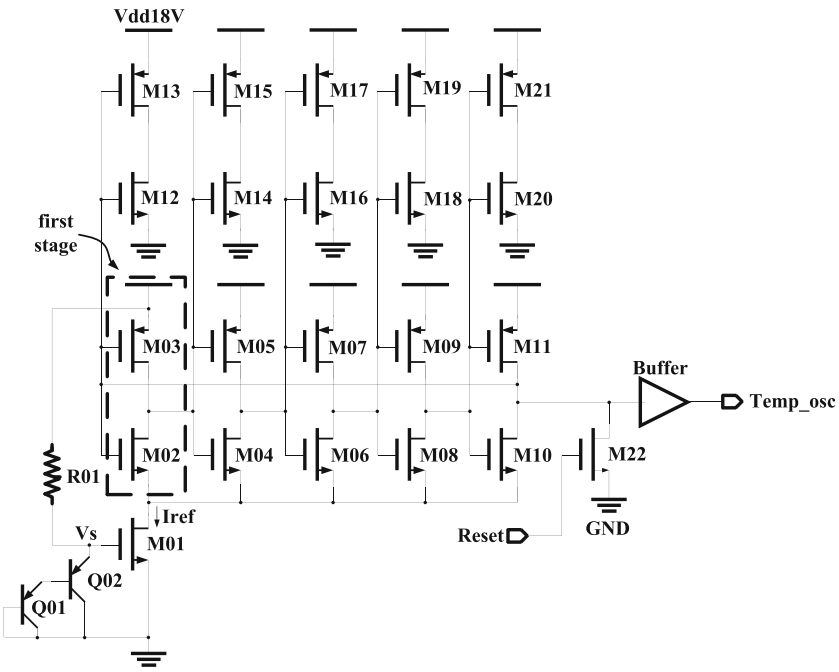


Figure 6 Schematic of temperature detector.

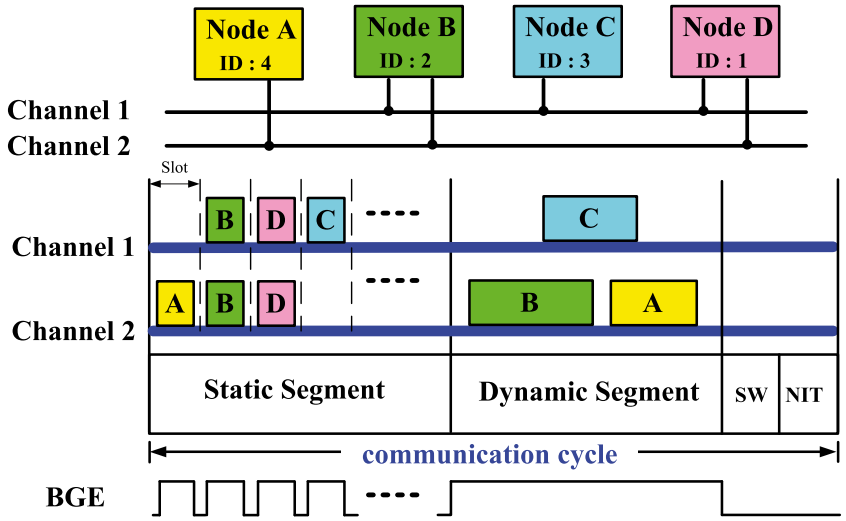


Figure 7 An example of the communication schedule in a FlexRay system.

3.1 Communication Controller Supervision (CCS)

Referring to Fig. 8, CCS is the main controller in BG to decide the function of every other block and deal with errors and commands from Host and CC. That is, CCS communicates with Host and CC to ensure correct operation state. When detecting an error in the communication schedule, CCS sends an interrupt signal to Host to request handling the error. CCS operation modes and transition conditions are described as follows. CCS process monitors the status of CC, and then determines transmission access to the communication medium. CCS controls the operation of blocks in BG and executes the commands received form the Host. CCS, Host, and CC communicate with each other to enter the corresponding operation state. As soon as the communication schedule error, the supervision error, or the operation state error is detected, CCS will generate an interrupt signal to notify Host. Figure 9 indicates an overview of CCS state transition[23].

The state transitions of CCS are described as follows:

1. Host generates a wakeup notification.
2. When BG detects any communication signal on the bus, CCS enters Silent state.
3. Host generates a notification signal for BG to supervise the Startup process.
4. Supervision error or Host command is notified.

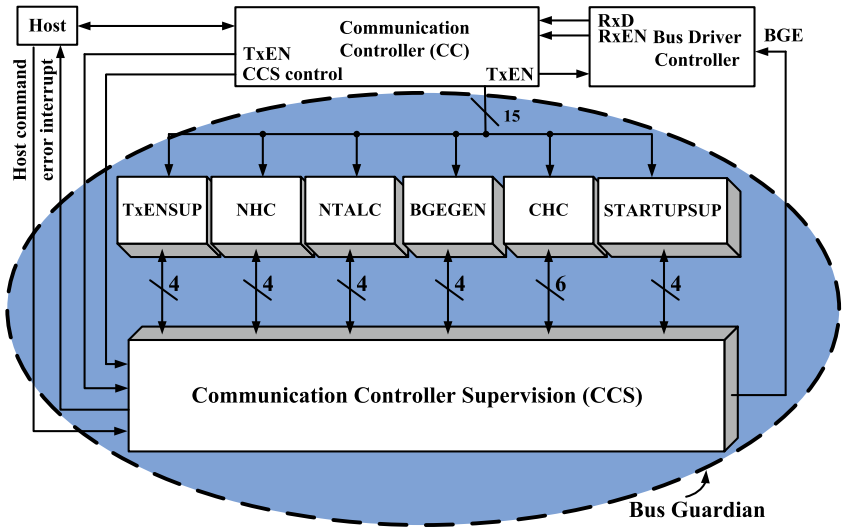


Figure 8 Architecture and interface of bus guardian.

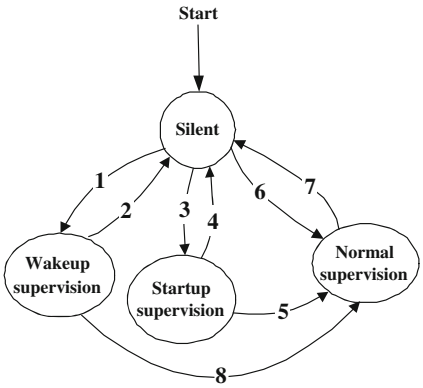


Figure 9 Overview of CCS state transitions.

5. ECU node has been included in a network, and BG has received a startup command from Host.
6. CC commands CCS to move into Normal supervision state from Silent state.
7. BG receives a CC or Host command to enter Silent state, or Supervision error is detected.
8. ECU node has been included in a network, and a wake up symbol, which will be described later with Fig. 11, has been recognized by BG.

Each state in Fig. 9 is explained as follows:

– **Silent:** Silent state is the starting state of BG, as well as the initial state when an error occurs. In this state, the communication to the access medium is disabled.
– **Wakeup supervision:** Figure 10 shows the Wakeup supervision timing diagram. BG supervises the wakeup behavior of CC. If no communication on the FlexRay bus is detected, BG then allows CC to transmit wakeup symbols (WUS), and Tx transmits wake up patterns on the channel. The wake up pattern is a sequential signal {Data_0, Idle, Data_0, Idle}, where each bit time must be longer than 4 μs, as shown in Fig. 11. In this state, BGE is enabled and confirmed to transmit a wakeup symbol when TxEN is enabled after a pre-defined timing parameter, pdCCSListenTimeout. If the TxEN is not enabled and the wakeup symbol is detected on the channel, BG will generate the interrupt signal to Host. However, when transmitting the wake up pattern, BG will stop the transmission after a pre-defined timing parameter, pdCCWakeupTimeout.

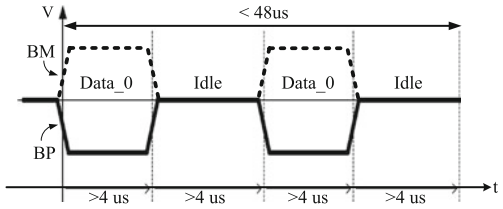
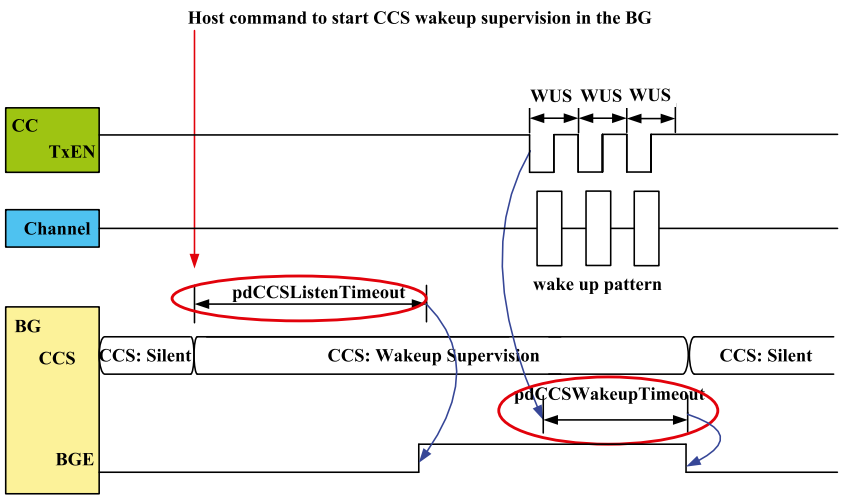


Figure 11 The wake up pattern.

– **Startup supervision:** BG supervises the startup behavior of CC. In this state, BG allows CC to transmit the collision avoidance symbol (CAS) through the channel when BGE and TxEN are both enabled. When BG detects an erroneous behavior of CC, the Silent state is entered.
– **Normal supervision:** In Normal supervision state, BG allows the access to the communication medium only for configured assigned slots. When BG detects an erroneous behavior of CC, the Silent state is entered.

Figure 10 Wakeup supervision timing diagram.



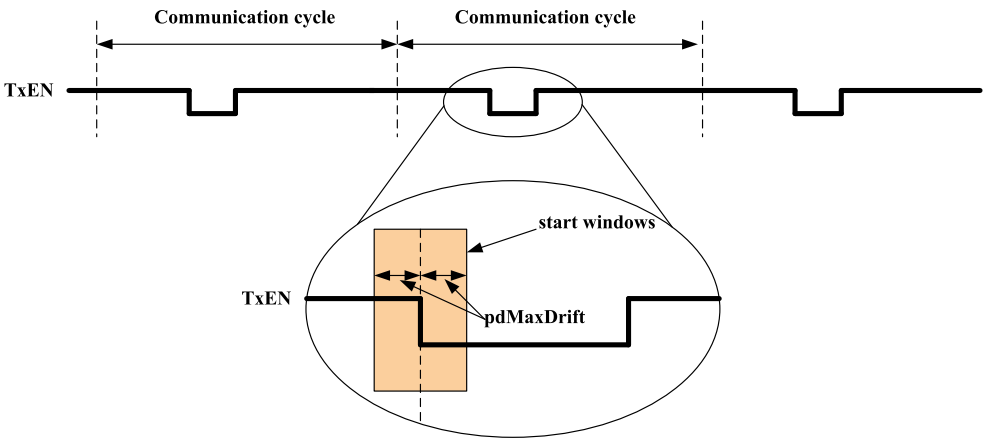


Figure 12 TxEN start window supervision.

3.2 TxENSUP (TxEN supervision process)

Referring to Fig. 8, the TxEN supervision process checks the behavior of the TxEN signal with respect to its sequence relationship with the BGE signal:

1. The BGE signal must be pulled high before any falling edge of TxEN signal.
2. The TxEN signal must be pulled high before any falling edge of BGE signal.

In addition, BG checks if there is only one active phase of the TxEN signal during one static segment to ensure that only one frame is transmitted by CC within one static segment. When the TxENSUP process detects more than one falling edges on the TxEN signal within one Static Segment, BG enters *CCS:silent* state. BG also checks if there is only one falling edge of the TxEN signal in one Dynamic Segment.

3.3 NHC

NHC in Fig. 8 checks if a decoded frame on a channel is received from CC or from another node. When the signal frame decoded on a channel is issued before the time constant, tFrameLength defined in [23], is expired, the valid frame is decoded from CC and the convey data of the header is checked.

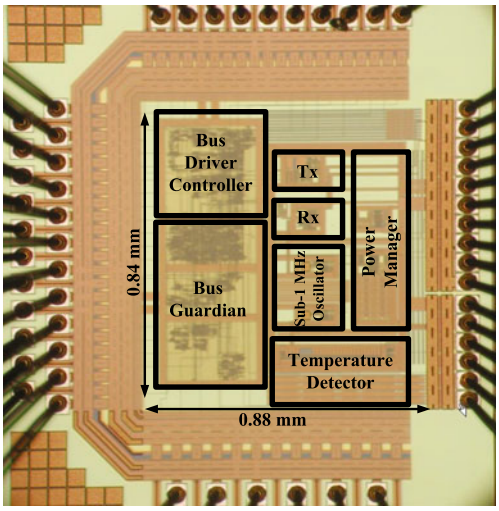


Figure 13 The die photo of the proposed FRT with BG.

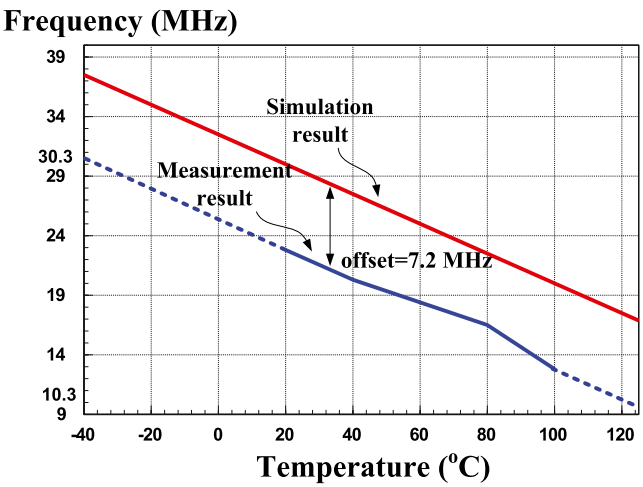


Figure 14 The simulation and measurement results of temperature detector.

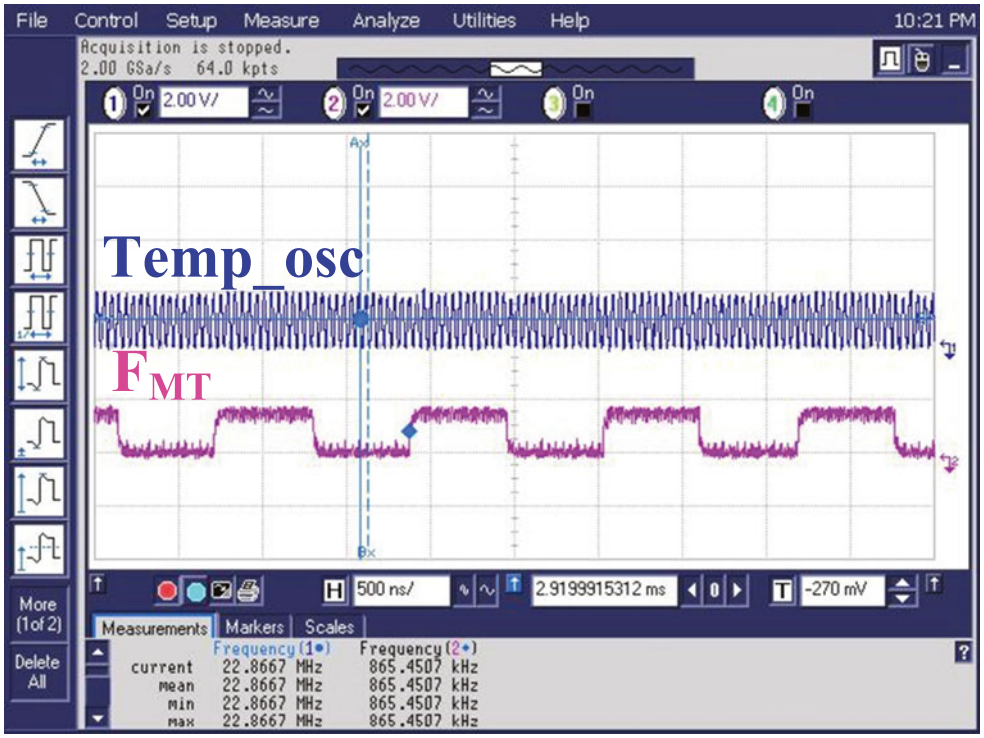


Figure 15 The measurement waveform of Sub-1 MHz Oscillator.

3.4 NTALC

Referring to Fig. 8, the function of NTALC is as follows. BG checks the length of the active phase in the TxEN signal. If the detected length of the TxEN active phase in not within a defined window, then the *CCS:silent* state is entered.

3.5 BGEGEN

BGEGEN in Fig. 8 is used to generate the BGE signal in the unit of MT, where MT is the period of F_{MT} generated by the Sub-1 MHz oscillator shown in Fig. 2, which was described in Section 2 early. When BG receives the command from CC, BG activates the BGE signal in Static Segment and Dynamic Segment.

3.6 CHC

The CHC process in Fig. 8 checks if a decoded frame on a channel is received from CC or from another node. If the decoded signal frame on a channel is transmitted before a specific time length, tFrameLength, is expired, the valid frame is from CC and the contents of the header are checked. In addition, the CHC process checks if CC is allowed to transmit a CAS.

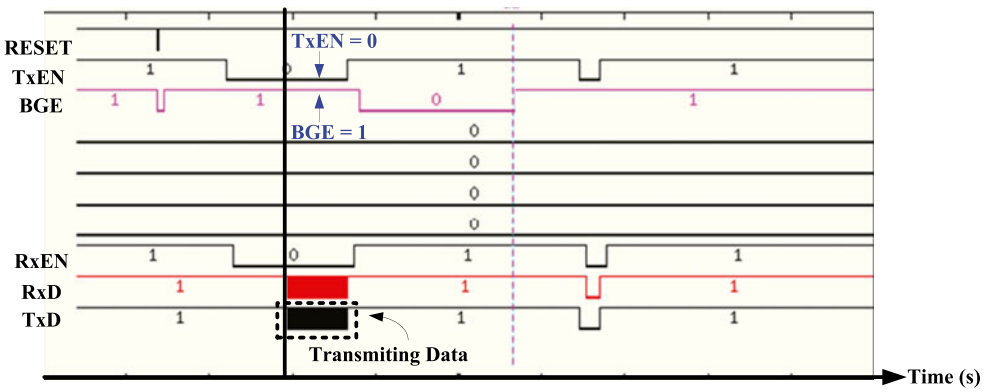


Figure 16 Measurement waveform of the BG (Agilent 16702B logic analysis system).

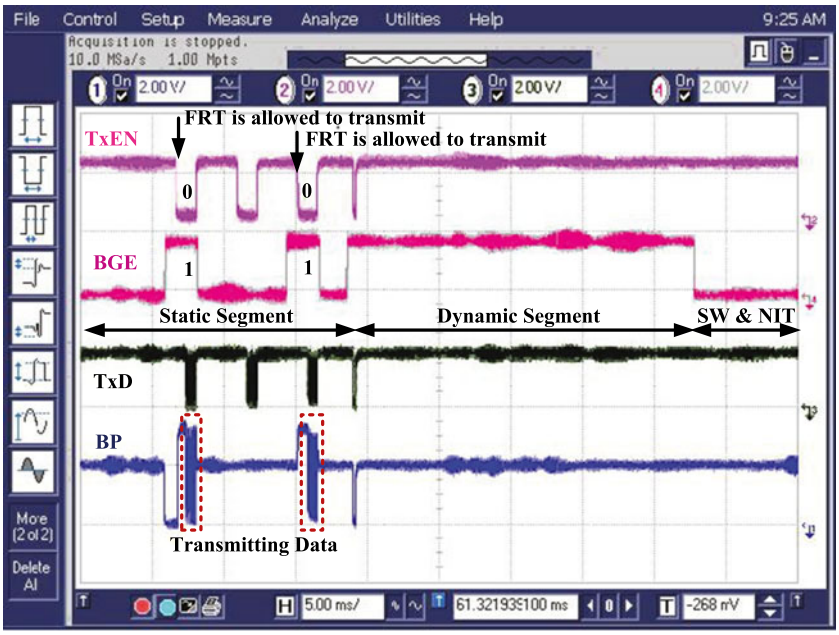


Figure 17 Measurement waveform when FRT transmits data in a communication cycle.

3.7 STARTUPSUP

STARTUPSUP is the process in Fig. 8 that allows BG to monitor the TxEN signal in the state of Startup supervision. The TxEN falling edge must be within a start window, which pdMaxDrift defined in [23], as shown in Fig. 12. The TxEN signal must be inactivated before the end of the Static Segment. If an error occur, BG enters the Silent state and generates an error interrupt to notify Host.

4 Implementation and Verification

The proposed FRT with BG is carried out by a typical 0.18 μm CMOS process. Figure 13 shows the die photo on silicon. The total core area is 0.88×0.84 mm^2.

Figure 14 shows the simulation and measurement results of Temperature Detector. Notably, Temperature Detector has an offset frequency, which is roughly 7.2 MHz, between simulation and measurement results. The frequency offset

Table 4 Comparison of FlexRay standards and the proposed Tx.

	FlexRay Tx specification	Measurement result of Tx
Absolute value of uBus, while sending (*)	600 ~ 2000 mV	990 mV
Absolute value of uBus, while Idle (*)	0 ~ 30 mV	< 30 mV
Transmitter delay, negative edge (***)	<100 ns	26.85 ns
Absolute value of uBus, positive edge (***)	<100 ns	29.64 ns
Transmitter delay mismatch	< 4 ns	2.79 ns
Fall time differential bus voltage (80 %→20 %)	3.75 ~ 18.75 ns	15.69 ns
Rise time differential bus voltage (20 %→80 %)	3.75 ~ 18.75 ns	17.65 ns
Throughput	10 Mbps	10 Mbps

(*) Load on BP/BM: 40Ω ||100 pF

(**) Load on BP/BM: 45Ω ||100 pF

(***) The measurement reaction time not include logic delay in BD

Table 5 Comparison of FlexRay standards and the proposed Rx.

	FlexRay Rx Specification	Measurement Result of Rx
Receiver delay, negative edge (*)	< 100 ns	5.68 ns
Receiver delay, positive edge (*)	< 100 ns	9.52 ns
Receiver delay mismatch	< 5 ns	< 3.84 ns
Idle reaction time	$50 \sim 400$ ns	207 ns
Activity reaction time	$100 \sim 450$ ns	211 ns
Data Rate	10 Mbps	10 Mbps

(*) The measurement reaction time not include logic delay in BD

might be caused by the heat sink effect of package and bond wire such that we can not directly measure the temperature of the die. Nevertheless, the slopes of the two parallel curves show the same negative temperature coefficient. Notably, the frequency range of 30.3 MHz $\sim$ 10.3 MHz corresponds to the temperature range of -40 °C $\sim$ $+125$ °C. Therefore, it is easy to detect if the operating temperature of the proposed FRT is in the range of -40 °C $\sim$ $+125$ °C by a reference clock, namely CLK.

Figure 15 shows the measurement waveform of Sub-1 MHz Oscillator, which generates a 865.45 KHz clock, F_{MT}, as the time unit MT for BG. In other words, MT is equal to 1.1555μs. Figure 16 shows the measurement waveform of BG. When TxEN and BGE signal are activated, FRT transmits and receives data on a FlexRay bus. Figure 17 shows a measured communication cycle using the proposed FRT. In Static Segment and Dynamic Segment, BG activates BGE signal to allow FRT to transmit data on bus, and then BG transmits TxD signal to bus through BP and BM.

Table 4 shows the comparison of measurement results between FlexRay specification and the proposed Tx. Table 5 shows the comparison between the required FlexRay V2.1 specification and the measurement result of Rx. Notably, all of the required Tx/Rx specs are met basing on our measurement results.

Table 6 shows the comparison of this work and several prior works. Because our design is implemented using a typical 0.18 μm CMOS process, the supply voltage of our design is lower than that of [5] and [6]. The disadvantage is that the absolute value of uBus is smaller than the prior works, but 990 mV is still larger than the requirement of FlexRay specification. In[10], the FlexRay transceiver did not have BG, Bus Driver Controller, Temperature Detector, and Sub-1 MHz Oscillator. Therefore, the proposed FRT with BG consumes more power dissipation compared with this work. Nevertheless, the proposed design is the only total solution for FlexRay FRT on silicon so far.

5 Conclusion

In this paper, we propose a robust FRT with BG for FlexRay network. BG is the key component in FRT to supervise the states of CC and activate Bus Driver. An FRT with BG must be performed high safety and reliability in a FlexRay network. The proposed design is implemented using a typical 0.18 μm CMOS process such that it can easily be integrated to a possible SOC solution. The measurement results justify our design is totally compliant with the FlexRay standards. Notably, Temperature Detector is good enough to detect temperature variation on chip. After the measurement, a digital processor in Host acquires the maximum frequency at -40 °C and minimum frequency $+125$ °C

Table 6 Comparison of the proposed FRT and prior works.

FlexRay Tx/Rx Specification	This work	[10]	[6]	[5]
Year	2012	2010	2010	2007
Technology	0.18 μm	0.18 μm	N/A	N/A
Absolute value of uBus while sending (*)	990 mV	1380 mV	4000 mV	1600 mV
Absolute value of uBus while Idle (*)	$\approx$30 mV	$\approx$ 30 mV	30 mV	25 mV
Transmitter delay negative edge (***)	26.85 ns	13.32 ns	50 ns	31 ns
Absolute value of uBus positive edge (***)	29.64 ns	13.29 ns	50 ns	32 ns
Transmitter delay mismatch	2.79 ns	0.029 ns	4 ns	1 ns
Receiver delay, negative edge (***)	5.68 ns	9.492 ns	80 ns	28 ns
Receiver delay, positive edge (***)	9.52 ns	9.065 ns	80 ns	30 ns
Receiver delay mismatch	3.84 ns	0.427 ns	5 ns	2 ns
Supply voltage	3.3 V	3.3 V	7 V	5.5 V
Power dissipation	53.04 mW	43.01 mW	315 mW	192.5 mW
Area	0.7392 mm^2	0.117 mm^2	N/A	N/A
Throughput	10 Mbps	10 Mbps	10 Mbps	10 Mbps

(*) Load on BP/BM: 40Ω ||100 pF

(**) Load on BP/BM: 45Ω ||100 pF

(***) The measurement reaction time not include logic delay in BD

from Temperature Detector, which are 30.3 MHz and 10.3 MHz, respectively. Therefore, the digital processor monitors the frequency of Temp_osc to check whether it is in the frequency range between 30.3 MHz and 10.3 MHz or not.

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Dr. Chua-Chin Wang received Ph.D. degree in electrical engineering from SUNY (State University of New York) at Stony Brook, USA, in 1992. He then joined Department of Electrical Engineering, National Sun Yat-Sen University, Taiwan, and became a full professor since 1998. He was Chairman of Department of Electrical Engineering, National Sun Yat-Sen University during 2009 2012. Dr. Wangs research interests include memory and logic circuit design, communication circuit design, and interfacing I/O circuits. Particularly, he applies most of his research results on biomedical, memories, consumer electronics, and wireless communication applications, such as implantable ASIC/SOC, DVB-T/H and NTSC TV circuits, low power memory, high speed digital logic, etc. He has won the Outstanding Youth Engineer Award of Chinese Engineer Association in 1999, and NSC Research Award from 1994 to 1999. In 2000. He co-founded Asuka Semiconductor Inc., which is an IC design house located in renowned Hsinchu Scientific Park, Taiwan, and became Executive Secretary in 2005. In 2005, he was awarded

with Best Inventor Award in National Sun Yat-Sen University, Taiwan. In 2006, he won Distinguished Engineering Professor Award of Chinese Institute of Engineers and Distinguished Engineer Award of Chinese Institute of Electrical Engineering in the same year. He also won Distinguished Electrical Engineering Professor Award of Chinese Institute of Electrical Engineers in 2007. In 2008, he won Outstanding Paper Award of 2008 IEEE Inter. Conf. of Consumer Electronics. In 2009, he again won Best Inventor Award. He was elevated to be Distinguished Professor of National Sun Yat-Sen University in 2010. He became IET Fellow in 2012.

Prof. Wang has served as program committee members in many international conferences. He was Chair of IEEE Circuits and Systems Society (CASS) for 2007 2008, Tainan Chapter. He was also the founding Chair of IEEE Solid-State Circuits Society (SSCS), Tainan Chapter for 2007 2008, and the founding Consultant of IEEE NSYSU Student Branch. He is also a member of the IEEE CASS Multimedia Systems & Applications (MSA), VLSI Systems and Applications (VSA), Nanoelectronics and Giga-scale Systems (NG), and Biomedical Circuits and Systems (BioCAS) Technical Committees. He is a senior member of IEEE since 2004. He was Chair of IEEE CASS Nanoelectronics and Giga-scale Systems (NG) Technical Committee for 2008 2009. Since 2010, he has been invited to be Associate Editors of IEEE Trans. on TCAS-I and TCAS-II. Currently, he is also serving as Associate Editor of IE-ICE Transactions on Electronics, and Journal of Signal Processing. Dr. Wang was General Chair of 2007 VLSI/CAD Symposium. He was General Co-Chair of 2010 IEEE Inter. Symp. on Next-generation Electronics (2010 ISNE). He was General Chair of 2011 IEEE Inter. Conf. on IC Design and Technology (2011 ICICDT), and General Chair of 2012 IEEE Asia-Pacific Conference on Circuits & Systems (2012 APCCAS).

Chih-Lin Chen was born in Taiwan in 1986. He received B.S. and M.S. degrees in electrical engineering from National Sun Yat-Sen University, Taiwan, in 2008 and 2010, respectively. He is currently working toward Ph.D. degree in electrical engineering at the National Sun Yat-Sen University. He is a student member of IEEE since 2010. His current research interests are VLSI design, high voltage mixed-signal circuit design, and automobile system design.

Gang-Neng Sung was born in Taiwan in 1981. He received B.S. degree in Department of Computer and Communication Engineering in National Kaohsiung First University of Science and Technology in 2004, and M.S. degree in Department of Electrical Engineering in National Sun Yat-Sen University in 2006. In 2010, he received Ph.D. degree in the Department of Electrical Engineering National Sun Yat-Sen University, Kaohsiung, Taiwan. He is currently working in National Chip Implementation Center (CIC), National Applied Research Laboratories (NARL), Hsinchu, Taiwan. His recent research interests include VLSI mixed-signal circuit design, low power design and car electronics.

Ching-Lin Wang was born in Taiwan in 1985. He received M.S. degree in electrical engineering from National Sun Yat-Sen University, Taiwan in 2009.

Chun-Ying Juan was born in Taiwan in 1982. He received M.S. degree in electrical engineering from National Sun Yat-Sen University, Taiwan in 2008. His recent research interest focuses on high voltage mixed-signal design.