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2-GHz 2×VDD 28-nm CMOS Digital Output Buffer with Slew Rate Auto-Adjustment Against Process and Voltage Variations*

Chua-Chin Wang†, Zong-You Hou‡ and Yu-Lin Deng§

Department of Electrical Engineering, National Sun Yat-Sen University, 70 Lian-Hai Rd., Kaohsiung, Taiwan
†*ccwang@ee.nsysu.edu.tw*
‡*blazesky@vlsi.ee.nsysu.edu.tw*
§*xx9900@vlsi.ee.nsysu.edu.tw*

U-Fat Chio¶ and Wei Wang‖

College of Electronics Engineering, Chongqing University of Posts and Telecommunications, Chongqing, P. R. China
¶*u.c.mo@ieee.org*
‖*wangwei@cqupt.edu.cn*

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A 2×VDD CMOS output buffer with process, voltage and leakage (PVL) detection mechanism is proposed such that slew rate is auto-adjusted to reduce the variations at different corners. To boost the driving current, low threshold voltage transistors are used instead of devices with typical threshold voltage in the driving transistor of output stage. More importantly, to prevent large leakage of those large low threshold voltage devices, leakage detection resistors are added at the gates of the always-on low threshold voltage transistors to clamp the leakage. The static power consumption is reduced when it is not activated. Another feature of the proposed design is that the gate-oxide leakage is also reduced by lengthening the driving transistors. Besides, all biases in the proposed design are generated from bandgap circuits such that not only is the variation caused by temperature drifting reduced, the area overhead and power dissipation are also minimized. The proposed design is carried out by using 28-nm CMOS process. The data rate proved by physical measurement is proved to be 2.0 GHz given 1.8/1.05 V supply voltage, namely, VDD or 2×VDD, when the proposed PVL detection as well as the compensation circuitry are activated.

Keywords: 2×VDD; CMOS; slew rate adjustment; PV variation and leakage detection; output buffer.

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†Corresponding author.

1. Introduction

By the demand of lower fabrication cost, lower voltage and lower power consumption, the CMOS technology has been developed toward nano-scale nodes for years. Nevertheless, a lot of PCB-based applications and systems are still equipped with chips fabricated by prior CMOS processes using various digital voltage levels, e.g., 5.0 V, 3.3 V or even 1.8 V. Thus, the digital data exchange among these chips becomes a topic. Particularly, the slew rate is one of the most important requirements for digital transmission and data exchange. Voltage level converter chips were then utilized to resolve this problem, which consume extra area and power in the PCB-based systems. To remove the level converters and reduce the PCB size, mixed-voltage buffers have been deemed as a better alternative.

Digital I/O interfaces have strict slew rate demand. For instance, the latest specification of double data rate fourth generation (DDR4) DRAM needs to comply high performance computing system (HPC), where minimum slew rate limitation is 4 V/ns. If the slew rate is too high, simultaneous switching noise (SSN) becomes a threat to jeopardize the signal integrity.[1] If the slew rate is too low, the time margin will violate setup time requirement.[2] Many researches in the past were proposed to resolve these slew rate problems. The stacked-transistor-based output stage and variation detectors are major approaches to resolve the variations of slew rate and increase reliability, respectively.[3–8] Meanwhile, a digital-based process detector has been reported to enhance the detection speed and make easier the detection design as well.[2] Many other PVT (process, voltage, temperature) detection methods were also proposed.[9–12] However, although PVT (process, voltage, temperature) variations are always discussed together as the all-corner variations, they have individual impact on the digital signal quality in reality.

However, an interesting phenomenon should be addressed. When the cost of the buffer design is an important consideration, the impact of (P, V, T) on the slew rate variation must be explored to prioritize these three major variation sources. Table 1 summarizes the result of Monte Carlo simulations (100 times), where the 1 V, TT, 25°C is considered as a baseline for fair comparison. One of the three variations, i.e., P, V, and T, is simulated at a time to see the impact that it generates. The temperature variation can be neglected from buffer designs if the cost of chip area is a primary design concern because the impacts of voltage and process on slew rate of

Table 1. Comparison of different factors to slew rate variation.

VDD (V)	Process corners	Temp. (°C)	ΔSL_{rise} (V/ns)	ΔSL_{fall} (V/ns)	Impact ratio (SL_{rise}/SL_{fall})
0.9–1.1×VDD	TT	25	2.08	1.93	4.1/3.64
1×VDD	All	25	1.78	1.74	3.63/3.28
1×VDD	TT	0–100	0.49	0.53	1/1

Table 2. Review of recent related works.

Reference	Topology	Compensation	Publication
[13]	comparator	only leakage	IEEE TCAS-II (2017)
[14]	PMOS threshold voltage detection	only leakage for SRAM	IEEE TVLSI (2016)
[15]	skewed inverter	PVT detection	Microelectronics J. (2015)
[16]	NMOS threshold voltage detection	PT detection	IEEE TCAS-I (2013)
[17]	2-stage threshold voltage detection	PVT detection	Microelectronics J. (2013)
this work	low threshold voltage, resistor clamp	PVL detection (Temperature is not included)	

rising and falling edges are found to be three times larger than temperature on slew rate of rising and falling edges.

1.1. *Review of prior related researches*

The research team of this work has very much focused on mixed-voltage I/O buffer and PVTL detection designs for many years. Table 1 summarizes individual technical contribution of each significant milestone so that the feature of this investigation can be exclusively highlighted.

Notably, all the references in Table 2 were not carried out by 28-nm technologies which have serious leakage issue compared with prior technology nodes. Leakage current results in the degradation of slew rate and power dissipation, which must be resolved in advanced nano-scale CMOS technology nodes. Furthermore, this investigation highlights the priortity of three variation sources, where temperature variation is found to be the least significant one.

Therefore, a cost-effective buffer design is demonstrated on silicon in this investigation, where the first process, voltage and leakage (PVL) detection and corresponding slew rate auto-adjustment designs for 28-nm mixed-voltage buffer designs are proved to be very performance competitive compared to all of the existing solutions. In short, the proposed design not only resolves leakage of digital output buffers in advanced nano-scale CMOS technology but also increases slew rate and enhances data rate to GHz level.

2. Nano-Scale 2×VDD Output Buffer

Figure 1 shows the Output Stage, Bandgap circuits, N-Process and P-Process Detectors, Voltage Detector and Digital Logic Circuit. DOUT is the digital signal to be transmitted outward and Clock is the main system clock. EN, Reset1 and Reset2 are three signals to activate PVL detection. The digital output voltage can be selected to be VDD or 2×VDD relying on the VDDIO. A total of six large driving NMOS and six driving PMOS in Output Stage are divided into two categories. One category comprises three NMOS and three PMOS driving transistors in response to

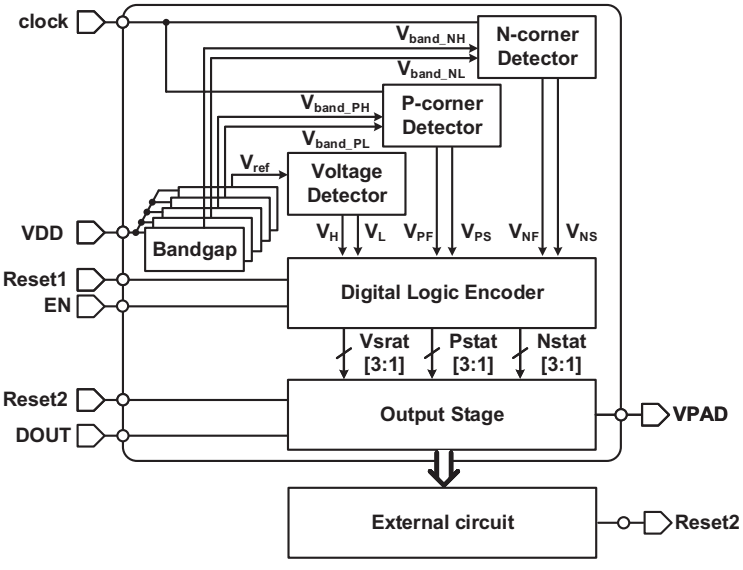

Fig. 1. 2×VDD digital output buffer.

the process detection outputs, while the other category consists of the rest of driving transistors in charge of the voltage variation. The function of the proposed buffer is briefed as follows:

(1) Voltage detection is realized by comparing two reference voltages in a PMOS string with a pre-defined bias voltage generated by another bandgap circuit. $V_{\rm H}$ and $V_{\rm L}$ will then be generated and coupled to Digital Logic Encoder.
(2) Clock with 50% duty cycle drives P-corner and N-corner Detectors at the same time. A ramping voltage is generated by each detector to compare with $V_{\rm ref}$ such that the delay of each detector will be monitored independently. $V_{\rm NS}$ and $V_{\rm NF}$ are generated by the N-corner detection, while $V_{\rm PS}$ and $V_{\rm PF}$ are generated by the P-corner detection opposite side.
(3) EN and Reset1 are externally generated signals to either deactivate or activate the proposed process and voltage detection and auto-adjustment circuitry.
(4) In fact, Digital Logic Encoder is a hard-wired circuit to encode the mentioned signals, including $V_{\rm PS}$, $V_{\rm PF}$, $V_{\rm NS}$, $V_{\rm NF}$, $V_{\rm H}$, and $V_{\rm L}$, into three categories of digital signals, Pstat[3:1], Nstat[3:1], and Vstat[3:1], to switch on or off the driving transistors correspondingly in Output Stage.
(5) Reset2 is responsible for compensation and leakage detection, where an External circuit is used to monitor the leakages of two always-on transistors in Output Stage and generate Reset2. If it is high, the leakage compensation mechanism is shut off.

2.1. *P-corner detector/N-corner detector*

The performance of the proposed buffer mainly relies on the process detection, which makes the slew rate auto-adjustment of the corresponding process variation feasible. As shown in Fig. 2, P-corner Detector consists of two comparators (i.e., CMP1 and CMP2), two DFFs and a P-skew cell. The aspect ratio (W/L) of pull-up PMOS device in the P-skew cell is relatively smaller than that of a regular inverter to accurately estimate the process variation impact upon the rise edge timing, while that of pull-down NMOS device therein is oppositely designed. In other words, P-skew cell is a skewed inverter with a long charging time. Because of the long pull-up device and the wide pull-down device, V_{C_P} at C_P will turn out to be a slow rising but fast dropping signal. Two thresholding voltages, namely, V_{P_H} and V_{P_L}, using CMP1 and CMP2, respectively, are then compared with V_{C_P}. The inverted outputs of these two comparators (V_{PF} and V_{PS}) are stored into DFF1 and DFF2, separately.

If PMOS is "Fast", V_{C_P} will be charged over V_{P_H} and V_{P_L} to make V_{PF} and V_{PS} both to be logic high. Therefore, V_{PF} and V_{PS} will be sampled as low at the rising edge of clock. If PMOS is in a "Typical" device with normal threshold voltage, V_{C_P} will be pulled up to stay between V_{P_H} and V_{P_L} such that V_{PF} and V_{PS} are separately registered with high (VDD) and low (GND). Last, if PMOS is a "Slow" device with high threshold voltage, V_{C_P} will be charged slower such that V_{C_P} cannot be pulled up over V_{P_H} and V_{P_L}. Figure 3 demonstrates a typical timing waveform for P-corner detection.

Figure 4 shows that the process detection circuit for NMOS device, consisting of two comparators (i.e., CMP3 and CMP4), two DFFs, two inverters and an N-skew cell. N-skew cell is also a skewed inverter. However, it is composed of a long pull-down device, a wide pull-up device, and a capacitor, C_N. The function of the N-corner Detector is very similar to that of the P-corner Detector. Figure 5 shows that a typical timing waveform of the N-corner Detector. All the above scenarios for N-corner and P-corner detection analysis are summarized in Table 3.

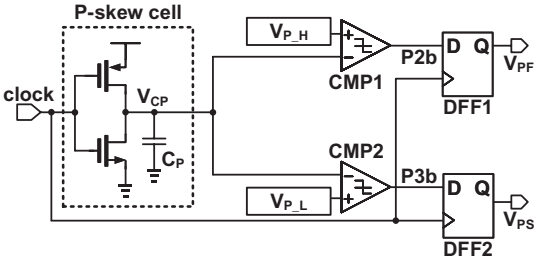

Fig. 2. P-corner detector.

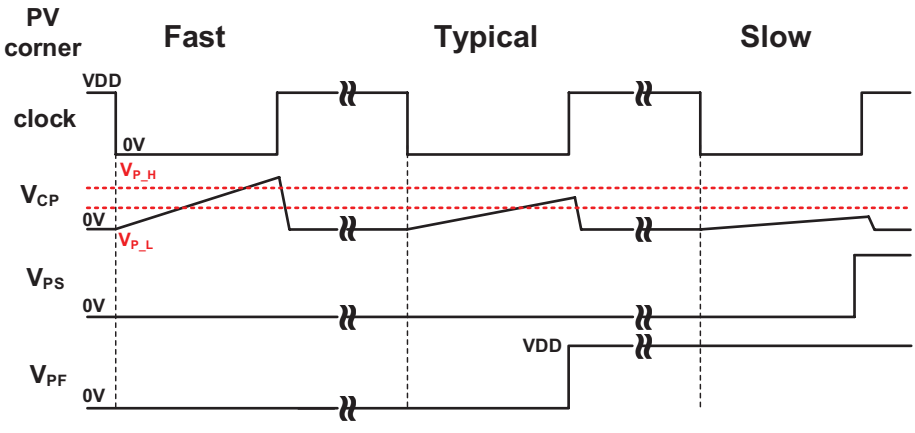

Fig. 3. Illustrative waveform for P-corner detector operation.

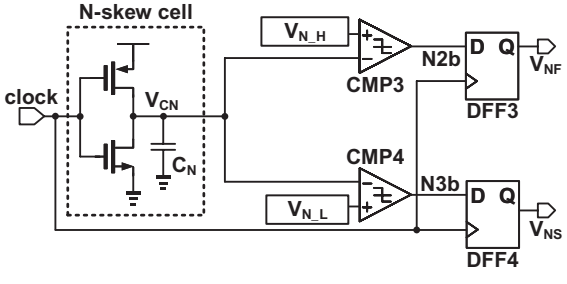

Fig. 4. N-corner detector.

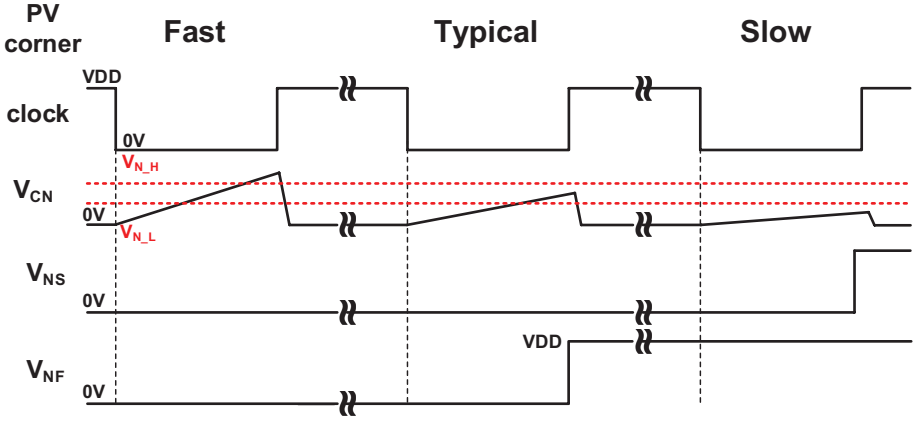

Fig. 5. Illustrative waveform for N-corner detector operation.

Table 3. Function table of process corner detectors.

N corner	V_{C_N}	V_{NF}	V_{NS}
Fast	$V_{C_N} > V_{N\_H} > V_{N\_L}$	low	low
Typical	$V_{N\_H} > V_{C_N} > V_{N\_L}$	high	low
Slow	$V_{N\_H} > V_{N\_L} > V_{C_N}$	high	high
P corner	V_{C_P}	V_{PF}	V_{PS}
Fast	$V_{C_P} > V_{P\_H} > V_{P\_L}$	low	low
Typical	$V_{P\_H} > V_{C_P} > V_{P\_L}$	high	low
Slow	$V_{P\_H} > V_{P\_L} > V_{CP}$	high	high

2.2. *Voltage detector*

With reference to Fig. 6, a Voltage Detector consisting of nine diode-connected PMOSs in a string is disclosed. These three categories correspond to three subranges from GND to VDD : GND $\sim V_L$, $V_L \sim V_H$, $V_H \sim$ VDD.[19] The variation of VDD between ±10% VDD can be directly sensed by such a configuration. Notably, all the PMOS transistors are designed with the same aspect ratio such that the influence, which is due to temperature and process variations, is auto-eliminated from each other. In other words, even though the resistance of diode-connected PMOS will drift given voltage variations, the generated reference voltages, V_H and V_L, are equally drifted. By thorough simulations, V_{ref} will be varied between −1.26% and +1.49% provided that VDD is suffering ±10% variation. Detailed function of this circuit is tabulated in Table 4.

2.3. *Digital logic encoder*

The Process Detectors and Voltage Variation Detectors generate all the mentioned signals, including V_{PF}, V_{PS}, V_{NF}, V_{NS}, V_H and V_L to Digital Logic Encoder. Notably, if

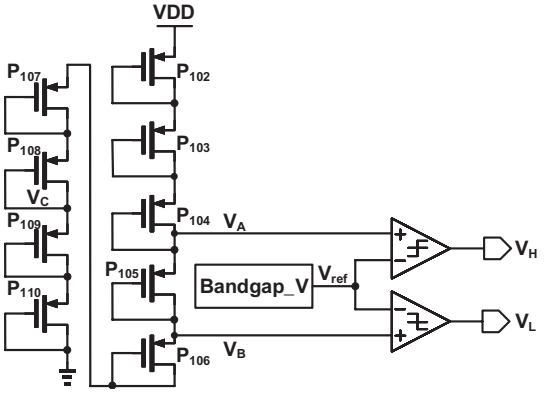

Fig. 6. Voltage variation detector.

Table 4. Function table of voltage variation detector.

Voltage	V_{H}	V_{L}
$\geq +10\%$ VDD	high	high
VDD	high	low
$\leq -10\%$ VDD	low	low

EN = high, output stage turns on all output driving current paths, namely, N201, N202, N203, N301, N302 and N303 or P201, P202, P203, P301, P302, and P303. Another issue is that the priority of signal EN is higher than that of Reset1. When Reset1 = low, the compensation mechanism is activated to carry out slew rate auto-adjustment. Then, Pstat[3:1], Nstat[3:1], and Vstat[3:1] are generated to activate different current paths in Output stage. On the contrary, when Reset1 = high, Pstat [3:1], Nstat[3:1], and Vstat[3:1] are all set as (low high high) regardless of whatever the outcomes of Voltage Detector and P/N-corner Detectors are. The truth table of Digital Logic Encoder is summarized in Table 5. Notably, the functionality of Voltage Variation Detector is the same as that of N-corner Detector provided that V_{NF}, V_{NS}, Nstat[3], Nstat[2], and Nstat[1], are replaced with V_{H}, V_{L}, Vstat[3], Vstat[2] and Vstat[1], respectively.

2.4. *Output stage*

Referring to Fig. 7, Output Stage comprises Pre-Driver, Vg1 level shifter, VDDIO detector/Vg2 generator, and Driving Transistors. The input signal Vstat[3:1], Pstat-[3:1], Nstat[3:1], and DOUT are coupled to Pre-Driver, which generates a total of 12 signals by a hard-wired logic circuit. V_{p1}, V_{p2}, V_{p3} and V_{n1}, V_{n2}, V_{n3} are coupled to Vg1 level shifter, while $V_{n201}, V_{n202}, V_{n203}$ and $V_{n301}, V_{n302}, V_{n303}$ are directly used as gate drives, individually, to N201, N202, N203, N301, N302, and N303. Notably, P201,

Table 5. Function table of digital logic encoder.

EN	Reset1	V_{PF}	V_{PS}	Pstat[3]	Pstat[2]	Pstat[1]
high	x	x	x	low	low	low
low	high	x	x	low	low	high
low	low	high	high	low	low	low
low	low	high	low	low	low	high
low	low	low	low	low	high	high
EN	Reset1	V_{NF}	V_{NS}	Nstat[3]	Nstat[2]	Nstat[1]
high	x	x	x	high	high	high
low	high	x	x	high	high	low
low	low	high	high	high	high	high
low	low	high	low	high	high	low
low	low	low	low	high	low	low

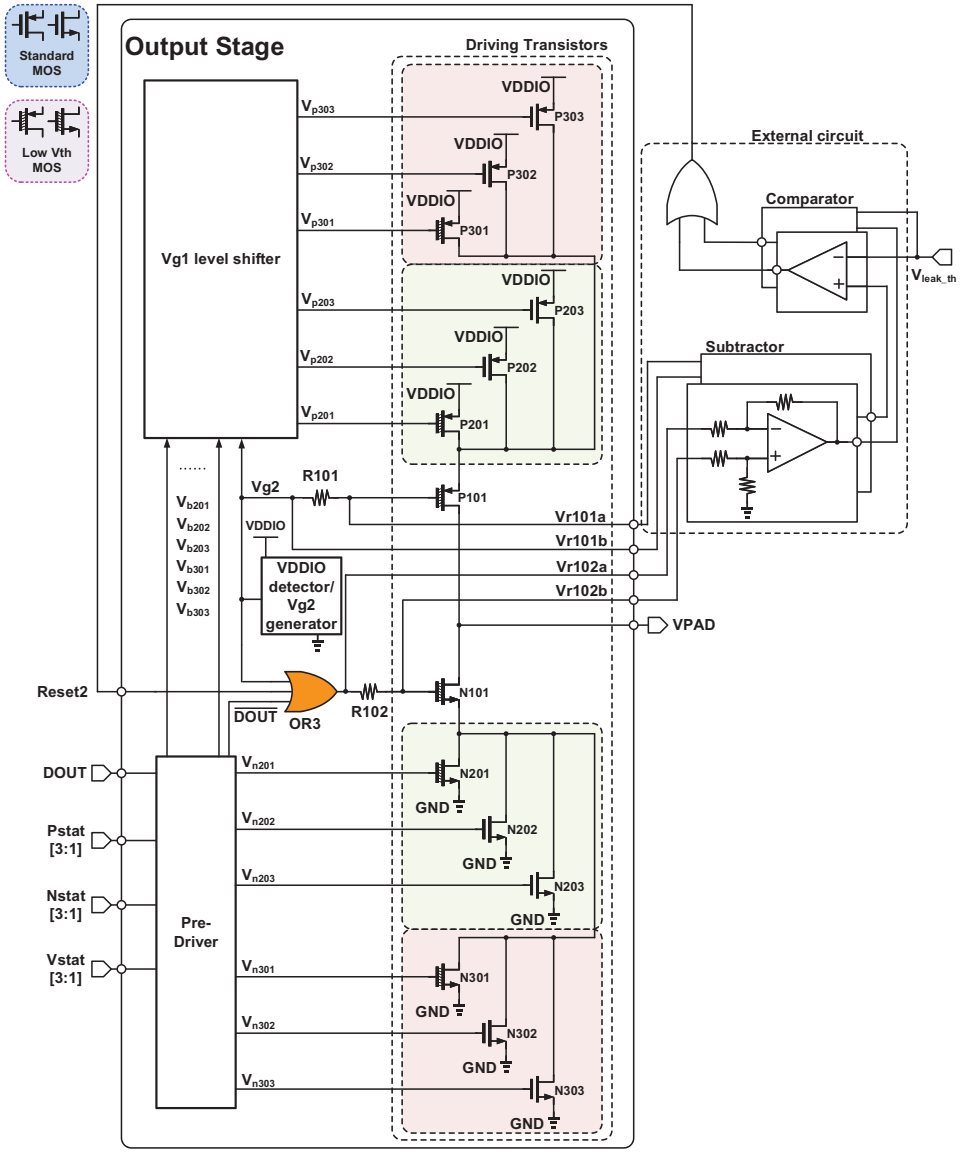

Fig. 7. The Output stage in Fig. 1.

P202, P203 and N201, N202, N203 generate individual driving currents in response to the process variation detection outcome. By contrast, P301, P302, P303, and N301, N302 and N303 are used to generate driving currents upon the outcome detection of voltage variations. Table 6 summarizes the voltage levels of all the signals in the Output Stage.

Table 6. Voltage levels of driving signals (x = a, b, c).

VDDIO (V)	V_{p20x}, V_{p30x} (V)	V_{g2} (V)	V_{n20x}, V_{n30x} (V)
1.05	1.05/1.8	1.05	1.05/1.8
1.8	0.0/1.05	0.0	0.0/1.05

2.4.1. *Leakage detection and reduction*

It is well recognized that known nano-scale CMOS processes suffer from significant leakage, e.g., 28-nm process. The leakage is particularly severe in an output buffer, where large driving transistors must be used to provide enough driving currents for off-chip loads. Otherwise, small driving current would result in poor slew rate to violate many I/O interfacing requirements. For the sake of providing large driving currents in the proposed buffer design, low threshold voltage devices are used to replace those regular devices in the basic current paths, which are P101, P201, N101, N201 and P301, N301, as shown in Fig. 7, since these two paths are always on.

The price to pay for using low threshold voltage devices is the enlargement of gate oxide leakage. It is even more severe in the low threshold voltage NMOS. Another fact is that most logic CMOS processes might not have a thick oxide layer to prevent such a leakage problem. Because N101 is an always-on low threshold voltage device, the NMOS is one of the major leakage sources. To reduce the unwanted power dissipation caused by this leakage, a three-input OR gate is added at the gate driving path of N101. The inputs of the OR gate are $\overline{\text{DOUT}}$, Reset2, and V_{g2}, such that N101 can be turned off in certain circumstances.

Regarding the generation of Reset2, namely the control signal of leakage compensation, an external circuit shown in the right-hand block of Fig. 7 is used. The voltage drops over R101 and R102, i.e., ($V\text{r}_{101b}$–Vr_{101a}) and (Vr_{102a}–Vr_{102b}), are sampled and coupled to individual OPA-based voltage subtractors. The output voltages of the subtractors are compared with a pre-defined $V_{\text{leak}_{\text{th}}}$ leakage threshold voltage. If either one is higher than $V_{\text{leak}_{\text{th}}}$, the output voltage of this external circuit, Reset2, will be pulled high. Otherwise, Reset2 stays low. Notably, R101 and R102, respectively, at the gates of P101 and N101, must be selected carefully. The resistances of these two monitoring resistors should be large enough to generate measurable voltage drops, but small enough not to attenuate the gate drives therewith.

In short, when Reset2 = high, the leakage compensation circuit is off. If Reset2 and V_{g2} are low such that VDDIO = VDD, V301 will be the same logic value as DOUT. Therefore, N101 is off to clamp the leakage path when DOUT is low. The leakage power will be reduced at least $\frac{1}{4}$ dramatically thanks to this extra leakage detection and reduction design.

2.4.2. V_{g1} level shifter

V_{g1} level shifter, as shown in Fig. 6, is an enhanced version of that in Ker's design.[7] The total of six identical voltage level shifters comprises this circuit to generate $V_{p201}, V_{p202}, V_{p203}$ and $V_{p301}, V_{p302}, V_{p303}$. When V_{g2} is high, all of the six generated outputs are boosted to [1.8 V, 1.05 V] from [1.05 V, 0 V], (namely, $V_{b201}, V_{b202}, V_{b203}$ and $V_{b301}, V_{b302}, V_{b303}$). Otherwise, the voltage level remains the same.

2.4.3. V_{g2} generator/VDDIO detector

This circuit is designed to carry out two functions, as shown in Fig. 9, i.e., V_{g2} generation and VDDIO detection.

- **VDDIO detection:** Voltage divider, which is the PMOS string at the left-hand side, generates the gate drives of P507 and P508. Note that P501 and N501 are not G-D-connected devices, which are used to create enough voltage drops and act as active current sources. If VDDIO is high enough to turn on P507 and P508, Vb will be pulled high to turn on N503. Thus, V_a is grounded to shut off N502 and latch on P508. Meanwhile, V_b is buffered to be V_c by two-tapered inverters.
- **V_{g2} generation:** One of the biggest challenges of nano-scale CMOS output buffer design is the small driving current. However, V_{g2} is used as an important bias in the entire circuit, it cannot be directly generated by a feature size inverter or buffer.

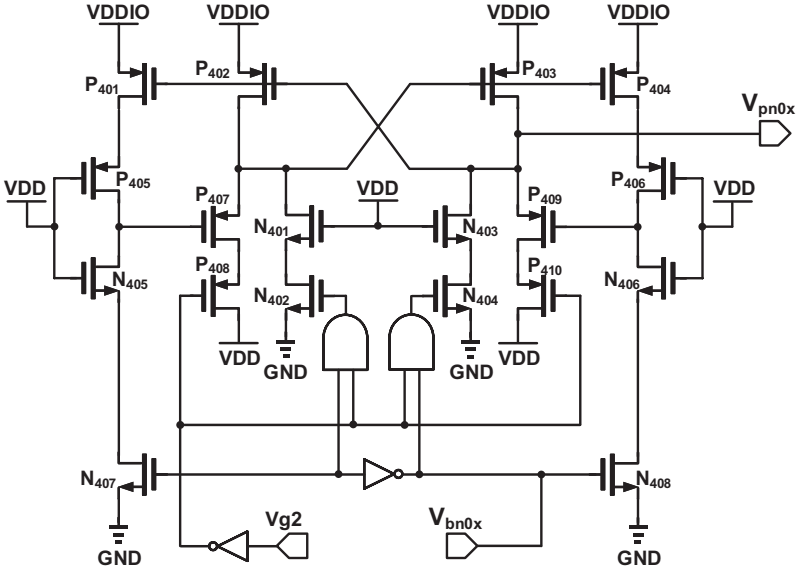

Fig. 8. V_{g1} level shifter.

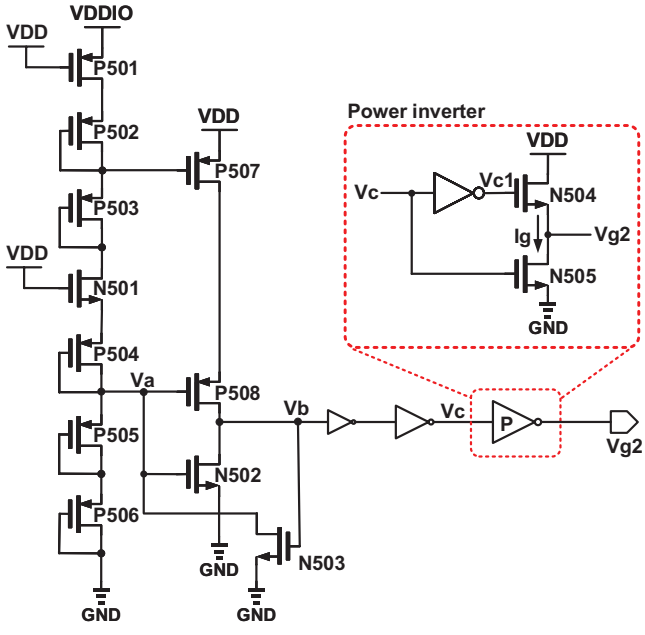

Fig. 9. VDDIO detector/V_{g2} generator.

The reason is that the small inverter or buffer will be affected by big load. The right-hand side of Fig. 9 shows that the proposed NMOS-based power inverter is made up of NMOS devices only to boost the output current of V_{g2} so that the loading problem is prevented.

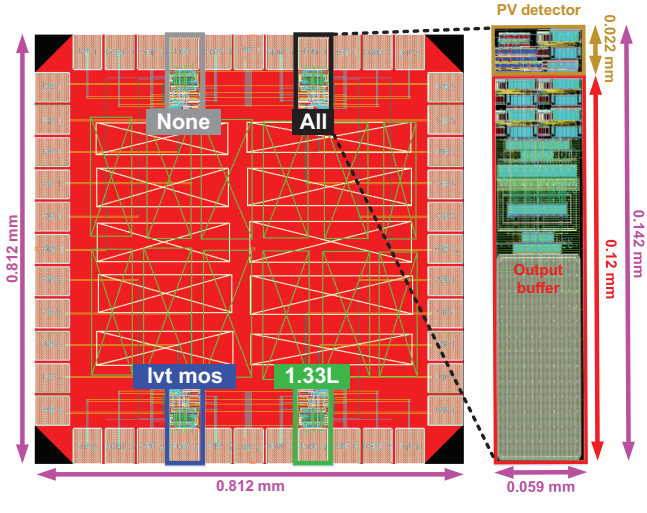

Fig. 10. Layout of the proposed output buffer.

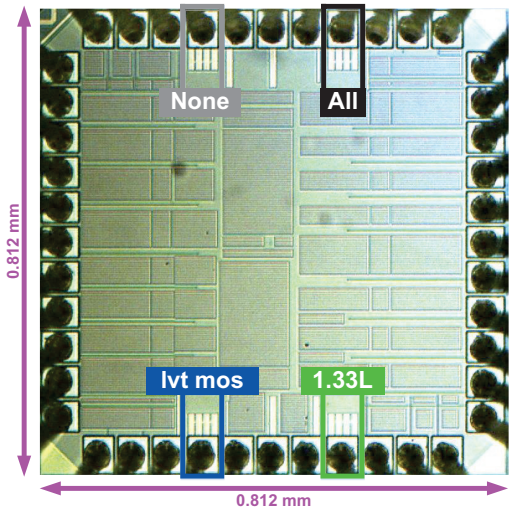

Fig. 11. Die photo of the proposed output buffer.

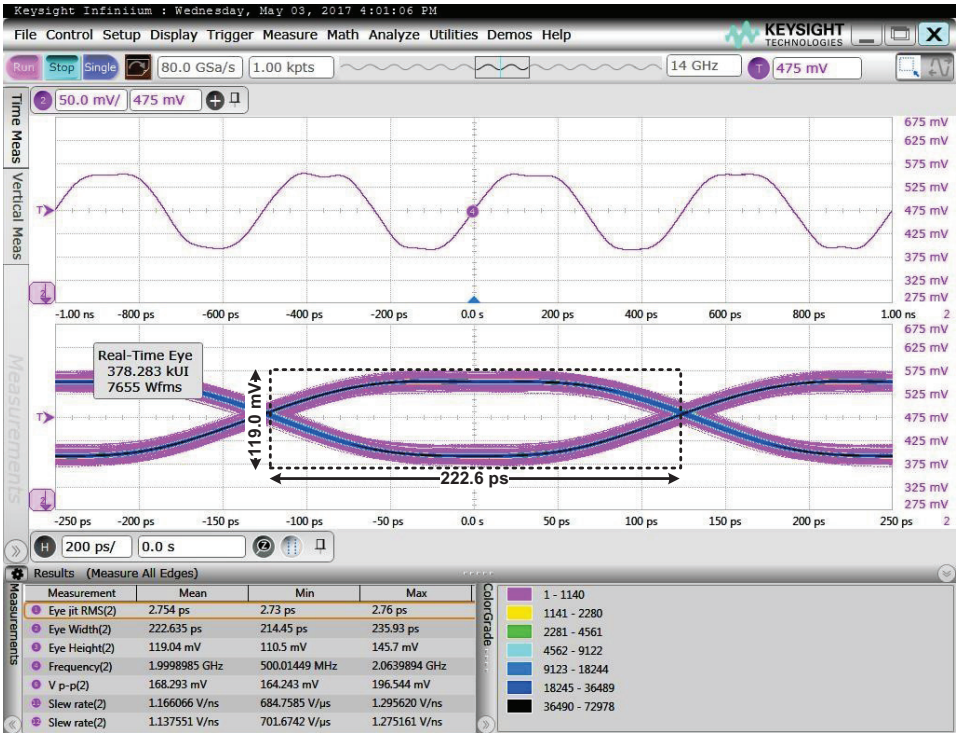

Fig. 12. Eye diagram with PV compensation given 1×VDD.

3. Implementation and Measurement

The proposed I/O buffer design is realized using TSMC 28 nm CMOS LOGIC Low Power ELK Cu 1P10M 1.05 and 2.5 V. Figures 10 and 11, respectively, show the layout and the die photo of the prototype on silicon, where a single I/O buffer circuit is only $0.142 \times 0.059\,\text{mm}^2$. The prototype chips were measured in Tainan Branch of CIC (Chip Implementation Center), Taiwan, using Analog Measurement System consisting of digital OSC (Keysight DSAV134A), logic analyzer (Agilent 16902B), etc. (*Note*: CIC is now renamed as TSRI, Taiwan Semiconductor Research Institute.) With reference to Figs. 12 and 13, which are screendumps generated by DSAV134A Infiniium V-Series Oscilloscope with Infiniium Oscilloscope Software,[18] the measurement of maximum data rate is 2.0 GHz when VDDIO = 1.8/1.05 V, respectively, with the activated PVL compensation. The performance comparison of the proposed design and several recent works is tabulated in Table 7. The proposed design attains the highest data rate with the least chip area among all solutions for 2×VDD buffer designs on silicon.

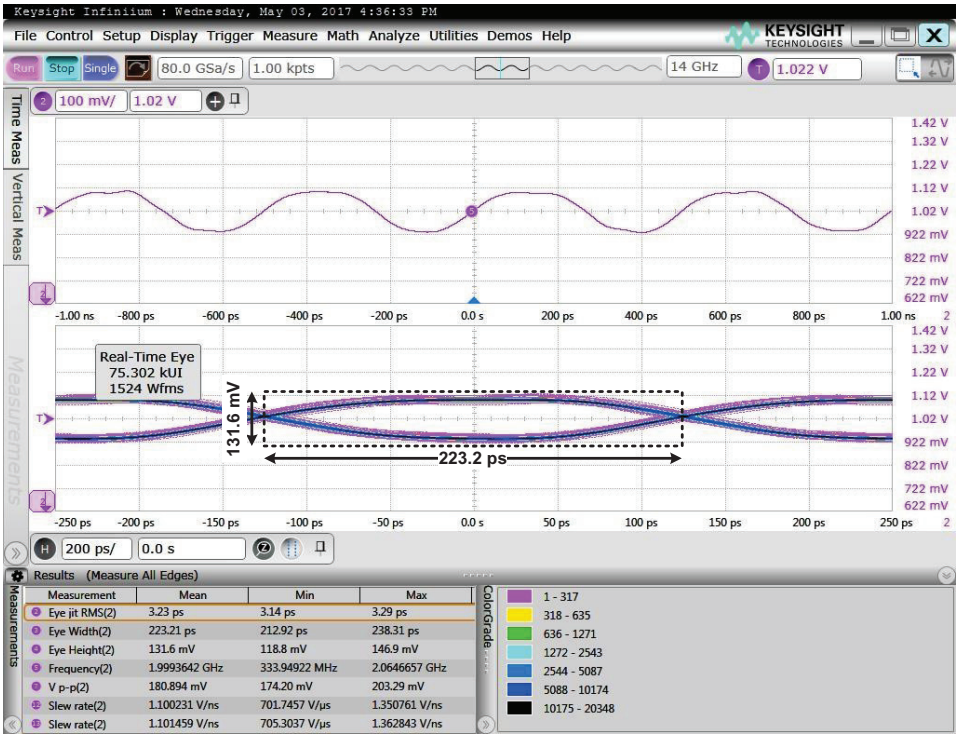

Fig. 13. Eye diagram with PV compensation given 2×VDD.

Table 7. Performance comparison of output buffers.

	Ref. 6 ISCAS	Ref. 7 TCAS-I	Ref. 8 EDSSC	Ref. 19 ISCAS	Ref. 20 TCAS-II	This work
Year	2013	2013	2014	2016	2018	2019
Process (nm)	40	90	90	90	65	28
Implementation	simulation	measurement	simulation	simulation	measurement	measurement
VDD (V)	0.9	1.2	1.0	1.0	1.2	1.05
VDDIO (V)	1.8/0.9	2.5	1.8/1.0	2.0/1.0	1.2	1.8/1.05
Lock Time	Tens of cycle	One cycle	≥ One cycle	One cycle	One cycle	One cycle
Maximum Date Rate (MHz)	460	200	330/500	800/500	1	2000/2000
Slew Rate Vriation Improvement (%)	6	37.5	N/A	33.9	33.3	55/58 (rise/fall)
Leakage compensation	NO	NO	YES	YES	NO	YES
Process Corner	All	Only TT FF SS	All	All	none	All
Detected Core area (mm^2)	0.013	N/A	0.024	0.020	0.0000075	0.0084
FOM[a]	1062	N/A	1042 (not included Slew Rate Variation Improvement)	67800	44400	654762

Note: [a]$\text{FOM} = \frac{\text{Max. Date Rate}\times\text{Slew Rate Variation Improvement}\times\text{Corners}}{\text{Core area}\times\text{Lock time}}$.

4. Conclusion

In this paper, a 28-nm 2×VDD output buffer is proposed. First of all, the impact of P, V and T, on slew rate is analytically demonstrated to highlight that the temperature detection and compensation is dispensable, since the impact of temperature on slew rate variation is around 10%. By contrast, the leakage poses significant impact on slew rate and power dissipation when nano-scale CMOS processes are used. Several critical designs have been proposed and verified on silicon to resolve the serious loss of performance, including low threshold voltage devices used in the driving transistors, the addition of leakage detection resistor at the gate of these low threshold voltage devices, and optimizing the length of the devices in the string. Therefore, not only is the slew rate variation reduced, but also the data rate is drastically enhanced to GHz level. When VDDIO = 1.8/1.05 V, respectively, the measurement of the proposed design on silicon is 2.0 GHz, which is fastest solution so far for mixed-voltage digital output buffer designs. The slew rate improvement is demonstrated to be at least over 50% regardless of VDD or 2×VDD data transmission mode, which is the best by far. To the best of our knowledge, this investigation is the first 28-nm CMOS mixed-voltage buffer design to demonstrate the GHz level data rate.

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