Transactions Briefs

Anti-PVT-Variation Low-Power Time-to-Digital Converter Design Using 90-nm CMOS Process

Chua-Chin Wang, Kuan-Yu Chao, Sivaperumal Sampath, and Ponnan Suresh

***Abstract*— One of the most important functional units in digital circuitry for synchronization and measurement is time-to-digital converter (TDC) which always requires higher resolution and accuracy. In this brief, a process, voltage, temperature (PVT)-variation-insensitive TDC featured with a PVT detector is proposed. The PVT detector takes advantage of another delay line with optimized locking conditions to differentiate PVT corners. The proposed TDC is physically realized using a 90-nm CMOS process. On-silicon measurement results demonstrate 30-ps resolution, <1.5 LSB INL/DNL, and 2.22 mW at 100 MHz and 1.2-V supply voltage.**

***Index Terms*— D flip-flip (DFF), process voltage and temperature (PVT), PVT corner detector, synchronization, time-to-digital converter (TDC).**

I. Introduction

Time-mode circuits where analog information is represented by the time difference between two digital signals offer a technology-friendly means to combat difficulties encountered in analog signal processing [1]. TDCs are devices commonly used to measure a time interval and convert this analog measure into digital (binary) output, e.g., generating the time of arrival for each incoming pulse. Thanks to this feature, TDCs have many applications, such as time of flight, radar ranging, and particle lifetime measurement (namely, lifetime measurements in atomic). In the 1970s, the high-energy physics as well as related circuits played major in nuclear science [2], including the TDC deployment in ADCs [3] and all-digital PLL [4], digital converters [5], to realize analog signals. The utilization of multistep architecture was carried out to achieve a subgate delay with higher resolution [6]. Notably, TDCs with fast conversion and high accuracy are the basic in these applications. However, quantization noise and delay drift caused by process voltage and temperature (PVT) variations have become a threat to the resolution and accuracy of TDCs. To resolve this problem, a new TDC design featured with a PVT detector is proposed to perform corner detection and auto-adjust the delay such that it is much less sensitive to PVT variations compared with existing TDCs.

II. TDC Design With PVT Detection

The proposed TDC with an anti-PVT-variation feature is shown in Fig. 1.

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Chua-Chin Wang is with the Department of Electrical Engineering, National Sun Yat-Sen University (NSYSU), Kaohsiung 80424, Taiwan, and also with the Institute of Undersea Technology (IUT), National Sun Yat-Sen University (NSYSU), Kaohsiung 80424, Taiwan (e-mail: ccwang@ee.nsysu.edu.tw).

Kuan-Yu Chao is with the Department of Electrical Engineering, National Sun Yat-Sen University (NSYSU), Kaohsiung 80424, Taiwan.

Sivaperumal Sampath and Ponnan Suresh are with the Department of Electronics and Communication Engineering, Vel Tech (Deemed University), Chennai 600054, India.

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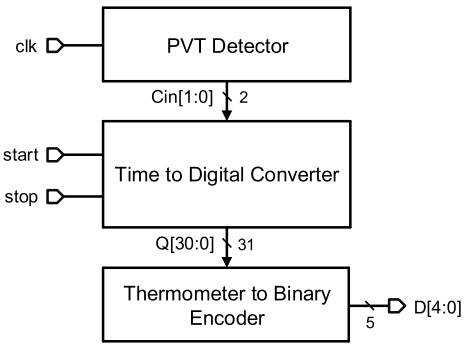

Fig. 1. Block diagram of the proposed TDC.

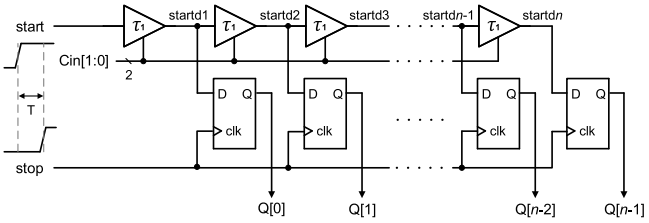

Fig. 2. Schematic of TDC in Fig. 1.

With reference to Fig. 1, "start" and "stop" are the beginning and the end of a timing event to be measured, respectively. They are given by an external device, e.g., stopwatch. Notably, the event to be sampled is assumed positive edge-triggered. The clk is used to drive The PVT detector, where 2-bit codes, namely, Cin[1:0], are generated. The TDC will then generate the digital code of the sampled timing event, which is assumed to be a 31-bit thermometer code Q[30:0] in our demonstration. The 31-bit thermometer code is finally converted into a 5-bit binary code D[4:0] by an encoder.

A. TDC Core Circuit

The core of the system is TDC, which is realized by a delay line as shown in Fig. 2. The "start" of the signal is initially raised and coupled to the input and then delayed for time T to approach "stop." Whenever the "start" ceases or it reaches toward "stop," the D flip-flip (DFF) output enables to "1" and otherwise, the output continues as "0." Namely, "T" is the time interval to be measured and converted.

A timing diagram example of TDC is depicted in Fig. 3, where in the time interval between "start" and "stop" is given as T in (1), the resolution of each delay element is τ_1 and length of thermometer code is denoted as N. The following relationship is used to estimate the time interval:

$$T = N \cdot \tau_1 + \varepsilon \tag{1}$$

where ε is the quantization error. However, if the number of delay elements $= n$, then the dynamic range DR $= (n + 1) \cdot \tau_1$. The values realized in this work are $\tau_1 = 30.0$ ps, $n = 31$, hence

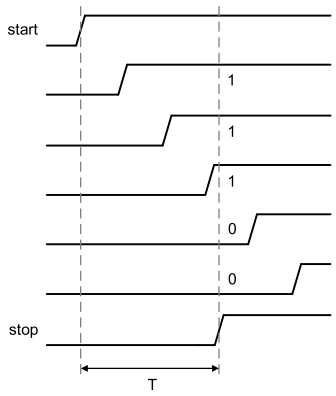

Fig. 3. Timing diagram example of our TDC.

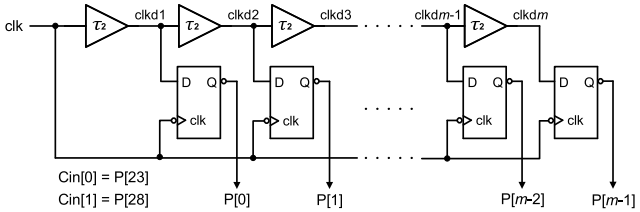

Fig. 4. Schematic of PVT detector.

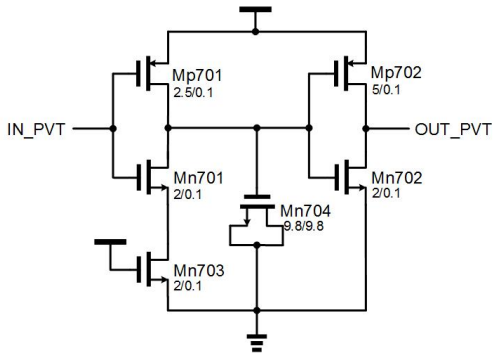

Fig. 5. Delay cell in PVT detector (W/L in μm).

DR = 960 ps theoretically and the binary output code length is 5. Notably, the resolution is heavily restricted by the process (90-nm CMOS in this work) to implement this circuit on silicon. As for the delay cell design is concerned, it is discussed later in the following text.

B. PVT Detector and Its Delay Cell

The PVT detector is used to monitor the status of ICs in a continuous manner and it works on the basis of the propagation delay of digital cells. The schematic of the PVT detector is shown in Fig. 4.

The delay cell in the PVT detector is shown in Fig. 5, which is not the same as the delay cell in the TDC delay line. The delay cell in the PVT detector is composed of Mp701, Mn701, Mp702, and Mn702. The most important design is that the always-on Mn703 ($\approx$ a resistor) and capacitor-formed Mn704 consist of an *RC* delay.

"clk" is the input of the PVT detector. This periodical signal is buffered by the delay cell chain, wherein each delay cell delays the "clk" by τ_2. A total of m delay cells are used to generate clkd1, clkd2, ..., clkd$m$, where $m = 31$ in this work. The m delayed pulse trains are latched by corresponding DFFs triggered by the original "clk" falling edge. By thorough simulation addressed in Section III

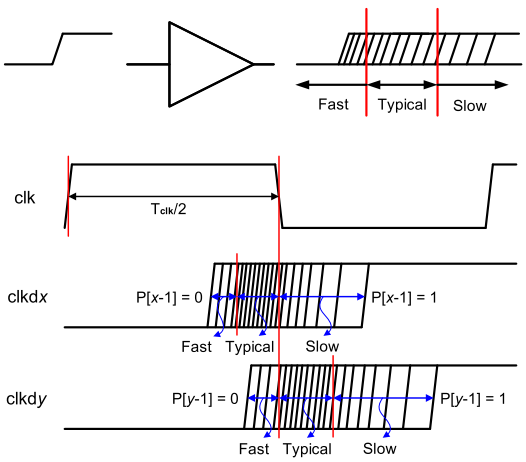

Fig. 6. Classification by stages 24 and 29 of the PVT detector.

TABLE I
CODES GENERATED BY THE PVT DETECTOR

PVT corner	Cin[1]=P[28]	Cin[0]=P[23]
Slow	1	1
Typical	1	0
Fast	0	0

(175 PVT corners and 1000 times Monte Carlo simulation), stages 24 and 29 of the delay line in PVT detector are found as the best thresholds to equally differentiate all the edges into three corner groups, i.e., slow, typical, and fast. Referring to Fig. 6, a typical locking scenario is illustrated. The rising edge is latched by clkd$x$ and clkd$y$ generated by the PVT detector. Notably, $x < y$, where $x = 24$ and $y = 29$ in this work.

1) If the PVT corner is "Fast," the falling edge of "clk" will "catch" the "high" level of both clkd24 and clkd29, to register "1 1" in their corresponding DFFs. The reason is the delay of each buffer is shorter in "Fast" corner. Notably, the outputs of the corresponding DFFs are the inverted Q. Therefore, P[23] = 0 = Cin[0], and P[28] = 0 = Cin[1], which is the entries in the last row of Table I.
2) If the PVT corner is "Slow" and then the delay of each cell will be longer, the falling edge of "clk" will "catch" the "low" level of both clkd24 and clkd29, to register "0 0" in their corresponding DFFs. Then, P[23] = 1 = Cin[0], and P[28] = 1 = Cin[1], which is the entries in the first row of Table I.
3) As for the "Typical" case, the falling edge of "clk" will "catch" the "high" level of clkd24 and "low" of clkd29 to result in P[23] = 0 = Cin[0], and P[28] = 1 = Cin[1], which are the entries in the second row of Table I.

In other words, the code generated by the PVT detector is tabulated as follows.

C. Delay Cell of TDC Core

Referring to Fig. 2 again, the delay cells in the delay line are governed by Cin[1] and Cin[0], which is directly coupled to outputs of the PVT detector such that the delay will be auto-adjusted. The schematic of the delay cells in the TDC core is shown in Fig. 7.

1) Slow (Cin[1], Cin[0]) = (1, 1) : Mn803 and Mn804 are turned on to shorten the delay.

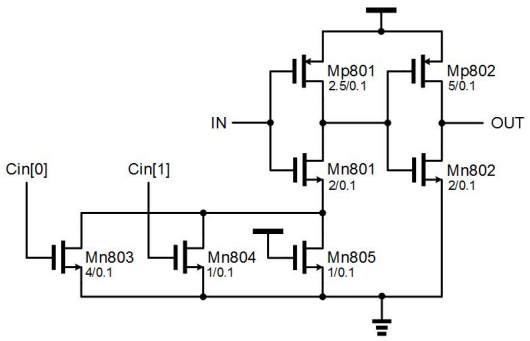

Fig. 7. Delay cell in TDC core (W/L in μm).

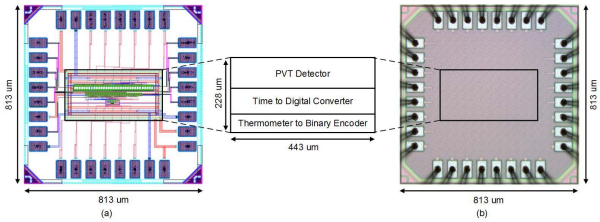

Fig. 8. (a) Layout of the proposed TDC. (b) Die photograph.

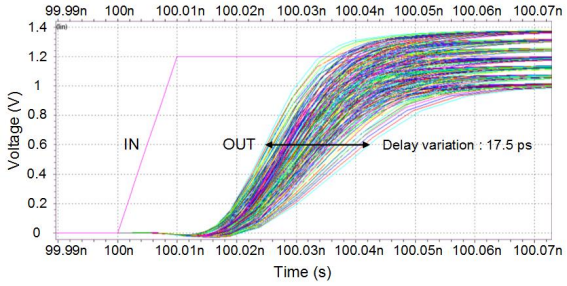

Fig. 9. Delay variation without PVT detection.

2) Typical (Cin[1], Cin[0]) = (1, 0): Mn804 is on for a normal case.
3) Fast (Cin[1], Cin[0]) = (0, 0): Mn805 is left alone to sink the current and hence the delay is increased.

Notably, the aspect ratio of all pull-down NMOSs is not the same. It is assumed that the sinking current, in Typical case, is the baseline. "Fast" case is designed to sink half of the baseline, while "Slow" case should be able to sink double. Thus, the aspect ratio of Mn801, Mn803, Mn804, and Mn805 is 2, 4, 1, and 1, respectively, to carry out the mentioned current-sinking ratios.

III. Implementation and Measurement

The proposed TDC with an anti-PVT-variation design is implemented using the TSMC mixed-signal/RF 1P9M low-power 90-nm CMOS process with ultra-thick (34 kA) top metal options. Fig. 8(a) and (b) shows the layout and the die images, respectively, where the chip area is 813 $\times$ 813 μm^2 and the active area is 228 $\times$ 443 μm^2. Notably, since the foundry service requires minimum metal density, the layout must be filled up with metal layers such that the die is fully covered by metal, which is why the details are not visible in the die photograph.

A. Post-Layout Simulations

All 175 PVT corners, including (SS, SF, TT, FS, FF), VDD ($-$15%, $-$10%, $-$5%, +0%, +5%,+10%, +15%), (0, 25, 50, 75, 100)°C,

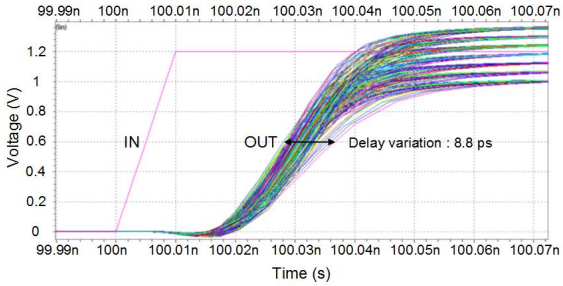

Fig. 10. Delay variation with PVT detection.

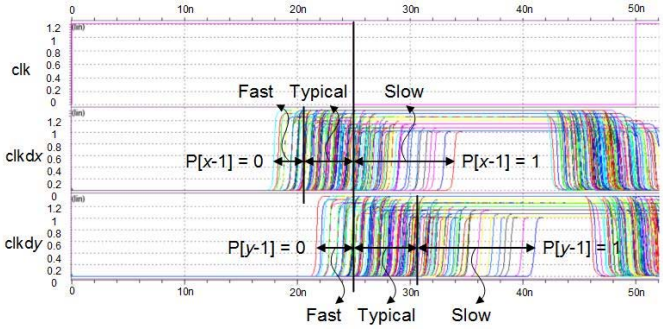

Fig. 11. Postlayout simulation of PVT detector.

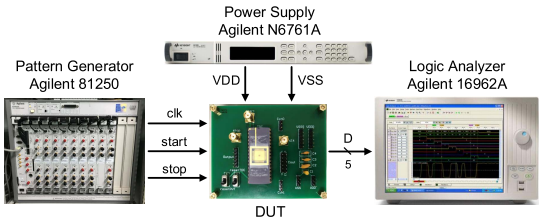

Fig. 12. Measurement setup.

are simulated using the Monet Carlo approach 1000 times to ensure the anti-PVT-variation robustness. Figs. 9 and 10 demonstrate the delay variations without and with PVT detection and self-adjustment. The delay variation is reduced from 17.5 to 8.8 ps, which is 49.71% reduction. All-corner post-layout simulations of the PVT detector are summarized in Fig. 11, which matches the theoretical prediction in Fig. 6.

B. Measurement of TDC Chips

A total of six prototype chips are measured, and the number of measurements is 63 times. Fig. 12 shows the measurement setup, which includes Agilent N6761A power supply, Agilent 16962A logic analyzer, and Agilent 81250 pattern generator along with the new TDC. Fig. 13 is the transfer function of this new TDC demonstrating the linearity between the delay and the output code. Although there is an offset error ($\approx$30 ps, 1 LSB) close to the origin, the linearity of the TDC is verified.

To ensure the accuracy of this design, DNL and INL measurement results with respect to the code generated are shown in Fig. 14(a) and (b), respectively. The worst DNL and INL are 1.17 and 1.5 LSB, respectively. Notably, if the offset error close to the origin, namely, code 0, is ignored, the DNL and INL are then reduced to be less than 0.2 and 0.5 LSB, respectively.

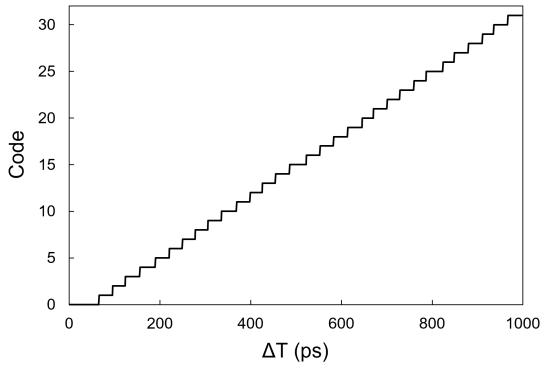

Fig. 13. Transfer function of the proposed TDC.

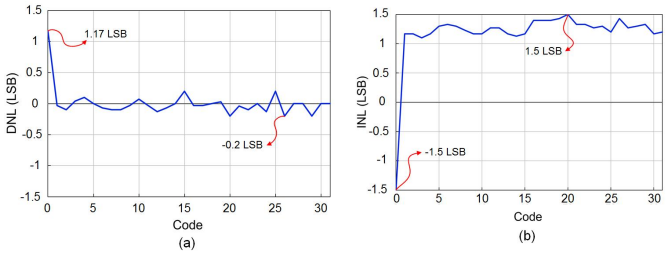

Fig. 14. Measurement of (a) DNL and (b) INL.

TABLE II
SUMMARY OF 63 MEASUREMENTS

	w/o PVT	with PVT
Delay range	24 ∼ 43 ps	25 ∼ 36 ps
Mean of delay	31.3 ps	30.0 ps
Deviation	5.3 ps	3.5 ps
Reduction of delay range	42%	
Reduction of deviation	34%	

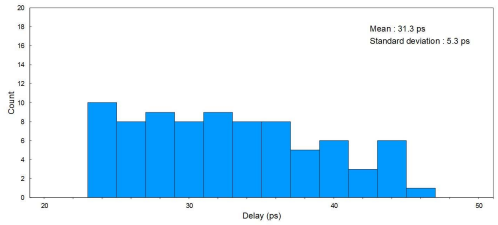

Fig. 15. Delay distribution without PVT detection by measurement.

The respective impact of voltage, process, and temperature variations upon circuit timing has been reported [11]. Not only the voltage variation is found to be the dominant one, its impact on circuit timing is around four times of that caused by temperature variation. Therefore, a total of seven different supply voltages are applied to the dies (chips): 1.02, 1.08, 1.14, 1.2, 1.26, 1.32, 1.38 V to verify the insensitiveness to PVT variations. Table II is the summary of these 63 measurements. Figs. 15 and 16 are the histograms of without/with PVT detection and auto-adjustment. The delay range is reduced from (43–24) to (36–25) ps, which is 42%, while the delay deviation is reduced from 5.3 to 3.5 ps, which is 34%.

The anti-PVT-variation performance given various supply voltages is plotted in Fig. 17. Table III shows the overall performance comparison of the proposed TDC versus several prior works.

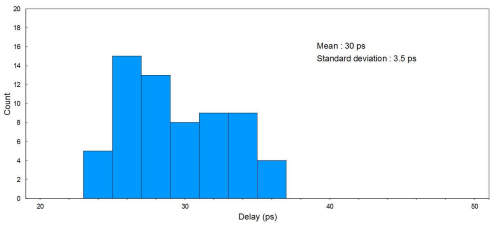

Fig. 16. Delay distribution with PVT detection by measurement.

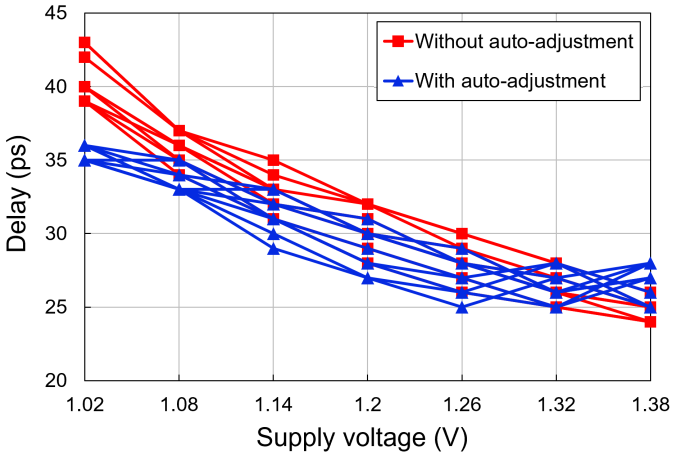

Fig. 17. Delay variation comparison given different VDD by measurement.

TABLE III
TDC PERFORMANCE COMPARISON

	ISSCS 2015[7]	ICCE 2016[8]	TCAS-II 2018[9]	MEJ 2018[10]	ours 2019
Arch.	Vernier	DLL	Ring OSC	Dual DLL	TDL
Process	65nm	65nm	130nm	180nm	90nm
Verifi.	Simul.	Simul.	Meas.	Meas.	Meas.
Resol.	6.15ps	2.0ps	43.2ps	15.0ps	30.0ps
DR	1260ps	1.0μs	N/A	500ns	997ps
clock	40MHz	N/A	100MHz	100MHz	100MHz
Power	2.5mW	69.7mW	1.72mW	75mW	2.22mW
DNL(LSB)	1.2	1	-1.0	1.7	1.17 (0.2)^a
INL(LSB)	2	1	-2.5	4	1.5 (0.5)^a
Δ delay	4ps (0.65LSB)	N/A N/A	6.4ps (0.15LSB)	10.0ps (0.67LSB)	11ps (0.37LSB)
FOM FOM^a	0.049	0.279	0.260	6.413	0.178 (0.047)^a

Notably, the FOM (Figure of Merit) is defined as follows:

$$\text{FOM} = (|\ \text{INL}\ | + |\ \text{DNL}\ |) \cdot \text{Power} \cdot \text{Resolution}. \tag{2}$$

Although our work attains the second-best FOM right after the work presented in 2015 ISSCS [7], the proposed TDC is superior in terms of lower power consumption and high clock frequency using a legacy CMOS process (90 nm versus 65 nm of [7]). If the offset error shown in Fig. 13 is ignored, then the errors at code "0" of DNL and INL in Fig. 14 are removed so that DNL and INL are reduced to be 0.2 and 0.5 LSB, respectively. FOM^a in Table III shows that our design outperforms [7] in such a scenario.

IV. CONCLUSION

The major contribution of this work is the self-adjustment capability provided by the PVT detector, where the generated PVT codes

are used to select the corresponding current-sinking path to reduce delay drift and achieve anti-PVT-variation performance.

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REFERENCES

[1] F. Yuan, "CMOS time-to-digital converters for mixed-mode signal processing," *J. Eng.*, vol. 2014, no. 4, pp. 140–154, Apr. 2014.

[2] Y. Tadokoro and T. Anayama, "Simple voltage-to-time converter with high linearity," *IEEE Trans. Instrum. Meas.*, vol. IM-20, no. 2, pp. 120–122, May 1971.

[3] M. Z. Straayer and M. H. Perrott, "A 12-bit, 10-MHz bandwidth, continuous-time $\Sigma\Delta$ ADC with a 5-bit, 950-MS/s VCO-based quantizer," *IEEE J. Solid-State Circuits*, vol. 43, no. 4, pp. 805–814, Apr. 2008.

[4] C.-M. Hsu, M. Z. Straayer, and M. H. Perrott, "A low-noise wide-BW 3.6-GHz digital $\Delta\Sigma$ fractional-N frequency synthesizer with a noise-shaping time-to-digital converter and quantization noise cancellation," *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 2776–2786, Dec. 2008.

[5] M. Park and M. H. Perrott, "A single-slope 80MS/s ADC using two-step time-to-digital conversion," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2009, pp. 1125–1128.

[6] B. Kim, H. Kim, and C. H. Kim, "An 8 bit, 2.6 ps two-step TDC in 65 nm CMOS employing a switched ring-oscillator based time amplifier," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Sep. 2015, pp. 1–4.

[7] X.-J. Zhang, K.-J. Cui, Z. Zou, and L.-R. Zheng, "A low-power coarse-fine time-to-digital converter in 65 nm CMOS," in *Proc. Int. Symp. Signals, Circuits Syst. (ISSCS)*, Jul. 2015, pp. 1–4.

[8] J.-H. Yu, M.-K. Park, and S.-W. Kim, "A 2 ps minimum-resolution, wide-input-range time-to-digital converter for the time-of-flight measurement using cyclic technique and time amplifier," in *Proc. IEEE Int. Conf. Consum. Electron. (ICCE)*, Jan. 2016, pp. 151–152.

[9] M. Perenzoni, L. Gasparini, and D. Stoppa, "Design and characterization of a 43.2-ps and PVT-resilient TDC for single-photon imaging arrays," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 65, no. 4, pp. 411–415, Apr. 2018.

[10] E. Jedari, R. Rashidzadeh, and M. Saif, "A PVT resilient short-time measurement solution for on-chip testing," *Microelectron. J.*, vol. 75, pp. 35–40, May 2018.

[11] C.-C. Wang, T.-Y. Tsai, Y.-L. Deng, and T.-J. Lee, "500 MHz 90 nm CMOS 2 $\times$ VDD digital output buffer immunity to process and voltage variations," *Circuits, Syst., Signal Process.*, vol. 38, no. 2, pp. 556–568, Feb. 2019.