

Article

A 40-nm CMOS Piezoelectric Energy Harvesting IC for Wearable Biomedical Applications

Chua-Chin Wang ^{1,2,*} , Lean Karlo S. Tolentino ¹ , Pin-Chuan Chen ¹, John Richard E. Hizon ³, Chung-Kun Yen ⁴, Cheng-Tang Pan ⁴ and Ya-Hsin Hsueh ⁵

¹ Department of Electrical Engineering, National Sun Yat-Sen University, Kaohsiung 80424, Taiwan; leankarlo.tolentino.ph@ieee.org (L.K.S.T.); billy0327@vlsi.ee.nsysu.edu.tw (P.-C.C.)

² Institute of Undersea Technology, National Sun Yat-Sen University, Kaohsiung 80424, Taiwan

³ Electrical and Electronics Engineering Institute, University of the Philippines Diliman, Quezon City 1101, Philippines; richard.hizon@eee.upd.edu.ph

⁴ Department of Mechanical and Electro-Mechanical Engineering, National Sun Yat-Sen University, Kaohsiung 80424, Taiwan; alden0113@gmail.com (C.-K.Y.); pan@mem.nsysu.edu.tw (C.-T.P.)

⁵ Department of Electronic Engineering, National Yunlin University of Science and Technology, Yunlin 64002, Taiwan; hsuehyh@yuntech.edu.tw

* Correspondence: ccwang@ee.nsysu.edu.tw

Abstract: This investigation presents an energy harvesting IC (integrated circuit) for piezoelectric materials as a substitute for battery of a wearable biomedical device. It employs a voltage multiplier as first stage which uses water bucket fountain approach to boost the very low voltage generated by the piezoelectric. The boosted voltage was further improved by the boost DC/DC converter which follows a predefined timing control directed by the digital logic for the said converter to be operated efficiently. TSMC 40-nm CMOS process was used for implementation and fabrication of the energy harvesting IC. The chip's core has an area of 0.013 mm². With an output of 1 V which is enough to supply the wearable biomedical devices, it exhibited the highest pump gain and accommodated the lowest piezoelectric generated voltage among recent related works.

Keywords: boost converter; CMOS; energy harvesting; piezoelectric; wearable



check for updates

Citation: Wang, C.-C.; Tolentino, L.K.S.; Chen, P.-C.; Hizon, J.R.E.; Yen, C.-K.; Pan, C.-T.; Hsueh, Y.-H. A 40-nm CMOS Piezoelectric Energy Harvesting IC for Wearable Biomedical Applications. *Electronics* **2021**, *10*, 649. <https://doi.org/10.3390/electronics10060649>

Academic Editor: Vincenzo Stornelli

Received: 22 January 2021

Accepted: 8 March 2021

Published: 11 March 2021

Publisher's Note: MDPI stays neutral with regard to jurisdictional claims in published maps and institutional affiliations.



Copyright: © 2021 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (<https://creativecommons.org/licenses/by/4.0/>).

1. Introduction

There is a huge demand for wearable sensors which are mainly used in monitoring health status of patients. Conventional batteries which are utilized as power supplies of these wearable sensors are being replaced. They may leak when they are not properly handled or packaged causing danger to the person. In addition, they cannot supply these wearables consistently due to limited battery capacity and the recharging requirement [1]. Moreover, they occupy too much space and add weight to the wearable sensor platforms [2,3]. Hence, they make the person wearing them feel uncomfortable. As a substitute for batteries in wearable sensor platforms, energy harvesting is being sought as a possible solution in providing power to these wearable sensors.

Meanwhile, human movements like feet and leg motion (walking and running), finger motion (writing and typewriting), and muscle contractions (heart, lung, and muscles) can bring an ample amount of wasted energy which can be harvested and converted to electricity. These biomechanical motions are commonly harvested by piezoelectric, electromagnetic, and triboelectric technologies [4,5]. Among the three energy harvesting technologies, piezoelectric is the most widely used and researched. Through the mechanical deformation of a piezoelectric material, an electricity is generated [4,6,7]. Some of the advantages of piezoelectric energy harvesting over the two technologies are higher energy density and output voltage [4,8]. The most widely known applications which utilized piezoelectrics are implemented in shoes [5,9]. More energy is generated by the piezoelectric when this is placed in shoes due to the weight exerted by the user standing on it and the

continuous activities made by the user by walking and running. However, the generated output voltage from the vibration of piezoelectric material is not enough to supply or drive an electronic system [10]. One advantage of piezoelectric is that they can be easily integrated and interfaced with electronic systems implemented in a chip for more enhanced energy harvesting; thus, output voltage is now boosted [4,8,11,12].

Many related works have been reported regarding piezoelectric energy harvesting ICs for typical and wearable biomedical applications. A 0.5- μm piezoelectric energy harvester was developed for wireless temperature monitoring which is capable of interfacing with wearables or implants where their data can be transmitted through the Internet (Internet of Things or IoT) [13]. It operates at a minimum input voltage of 0.51 V but generates voltage of only 3 V. In [8], they used a 130-nm CMOS full-bridge rectifier as energy harvester since the the voltage drop across the full-bridge rectifier is lower than the traditional off-chip diode. The voltage conversion ratio or pump gain is 0.987 while the output power is 10.7 μW . Meanwhile, a piezoelectric energy harvesting circuit was developed that serves as supply to the wearable cannula for infant respiratory monitoring [14]. It has a pump gain of 0.987 but a higher output power of 11.1 μW . A buck-boost converter was used for an input voltage of 0.54 V amplitude [15]. Its generated output voltage and power are 3.3 V and 57 mW, respectively. A 0.18- μm piezoelectric energy harvester for wireless sensor nodes was proposed [16], where its possible generated output power and voltage are 94 μW and 1.8 V for an input voltage of 1 V. Lastly, a study in [17] presented a 0.5- μm CMOS vibrational energy harvester that has a pump gain of 3 but only operates at a minimum input voltage of 1 V.

In this study, a piezoelectric made from polyvinylidene fluoride (PVDF) was used because it is flexible which makes it to be wearable, comfortable, and non-intrusive or unobtrusive [14] to the users than the brittle piezoelectric made from lead zirconate titanate (PZT) [18]. The said PVDF as shown in Figure 1 has a wire diameter of 10 μm and wire length of 1 mm. It has a vibration frequency of 6.67 Hz and maximum output voltage of 45 mV. Its output voltage was increased to 120 mV through series connection of the fibers. It was placed on the insole of the shoe.

Based from the previous works presented, none of them have developed an energy harvesting circuit that can accommodate an input voltage below 0.5 V. Previously, we proposed a PVDF film-based energy harvesting circuit [3] for the detection of missing children and elderly using a Bluetooth low energy (BLE) transceiver which requires at least 1 V power supply. Post-layout simulations were made for the evaluation of the said energy harvesting circuit with no chip implementation, measurements, and theoretical analysis conducted. In this paper, an energy harvesting circuit for low voltage PVDF piezoelectric which accommodates at least 120 mV-amplitude input voltage was realized that can be utilized for wearable biomedical applications. TSMC 40-nm CMOS process was used for implementation and fabrication of the energy harvesting IC. The fabricated chip was embedded inside the heel of the shoe for testing. It generates a maximum voltage of 1 V which is enough to drive and supply low-power and low-voltage wearable sensor platforms and systems.

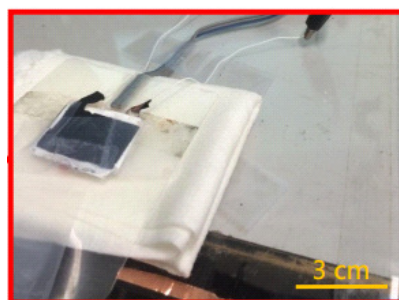


Figure 1. Polyvinylidene fluoride (PVDF) piezoelectric used in the proposed energy harvester.

2. System Architecture of Energy Harvester

The piezoelectric energy harvesting circuit architecture for wearable biomedical applications is shown in Figure 2. It is composed of AC/DC Converter, Voltage Monitor, and DC/DC Converter, which will be presented in the following subsections.

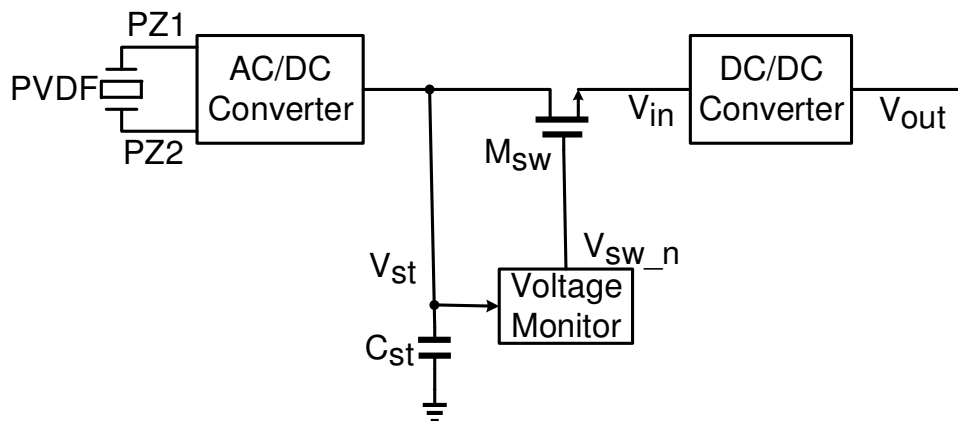


Figure 2. PVDF energy harvesting circuit.

2.1. AC/DC Converter

In piezoelectric material energy harvesting circuits, AC/DC converters are needed. There are many different implementations for AC/DC converter circuits, e.g., [19]. However, due to efficiency and simplicity in practical applications of PVDF energy harvesting circuit for wearable biomedical devices, Voltage Multiplier or Charge Pump as shown in Figure 3 was selected in this study as AC/DC Converter in Figure 2. This 5-stage Voltage Multiplier is widely used in energy harvesting to convert AC to DC signals. It is a switched capacitor which elevates the lower voltage to a higher voltage value. Moreover, it can provide a preliminary boost to facilitate the design of the DC/DC Converter, thereby alleviating the problem of too small input voltage in the subsequent DC/DC Converter design. Because the PVDF film’s output voltages at PZ1 and PZ2 are very low, a low V_{th} transistor is utilized reducing the voltage drop and boosting the voltage efficiently.

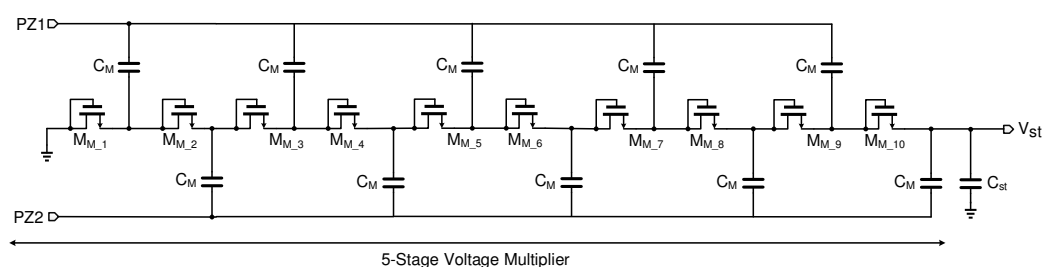


Figure 3. Voltage multiplier or charge pump as AC/DC converter.

2.2. Voltage Monitor

Since a very low output voltage is generated by the PVDF film, energy must be stored at C_{st} first. Then, the next stage will be driven by the large stored energy in C_{st} . As shown in Figure 4, V_{st} is monitored by a CMOS-based Schmitt trigger [20]. When $V_{st} >$ high switching voltage V_{SPH} , the power MOS switch M_{sw} in Figure 2 is switched on. At this moment, the DC/DC converter is started by an enable signal ($V_{sw_n} = 1$). When $V_{st} <$ low switching voltage V_{SPL} , a disable signal is sent by the Schmitt trigger ($V_{sw_n} = 0$) to turn off the DC/DC converter and restore energy in C_{st} .

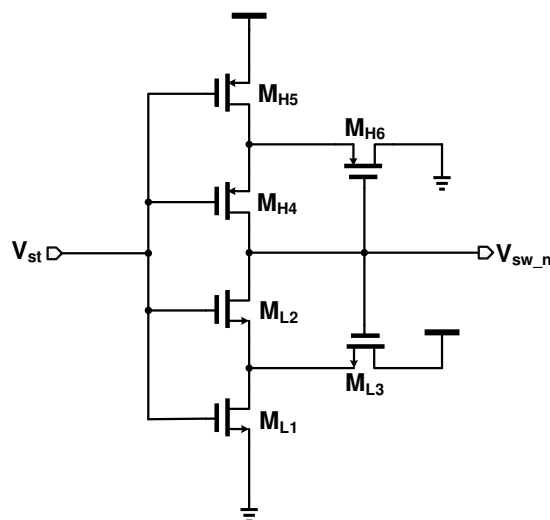


Figure 4. Schmitt trigger as voltage monitor.

2.3. DC/DC Converter

The Boost DC/DC Converter is displayed in Figure 5 [21]. It is composed of Digital Logic, On-time Mode Generator (T_{on} Generator), Off-time Mode Generator (T_{off} Generator). The PMOS switch P_{sw} is used to replace the diode which has lower voltage drop and better efficiency; hence, the said converter is a synchronous type instead of a diode architecture. Because of very low output voltage of PVDF, the bucket fountain method [22] is used in which the energy is kept in C_{st} until it is fully charged to the preset voltage value, and then the second stage boost is used to drive the wearable biomedical device. The Voltage Monitor is used to determine whether the stored voltage is sufficient. If the stored voltage is large enough, the power transistor (M_{sw}) in Figure 2 is turned on, and a large enough voltage is generated through the DC/DC converter to drive the wearable biomedical device. The system is in standby state waiting for the next startup. When the Voltage Monitor sends an enable signal ($V_{sw_n} = 1$), the DC/DC converter will now start to operate. S_1 , S_2 , and S_3 are generated by the Digital Logic. $\overline{S_2}$ and $\overline{S_3}$ are denoted by S_{2_b} and S_{3_b} , respectively. A comparator is interfaced to the Digital Logic for output adjustment.

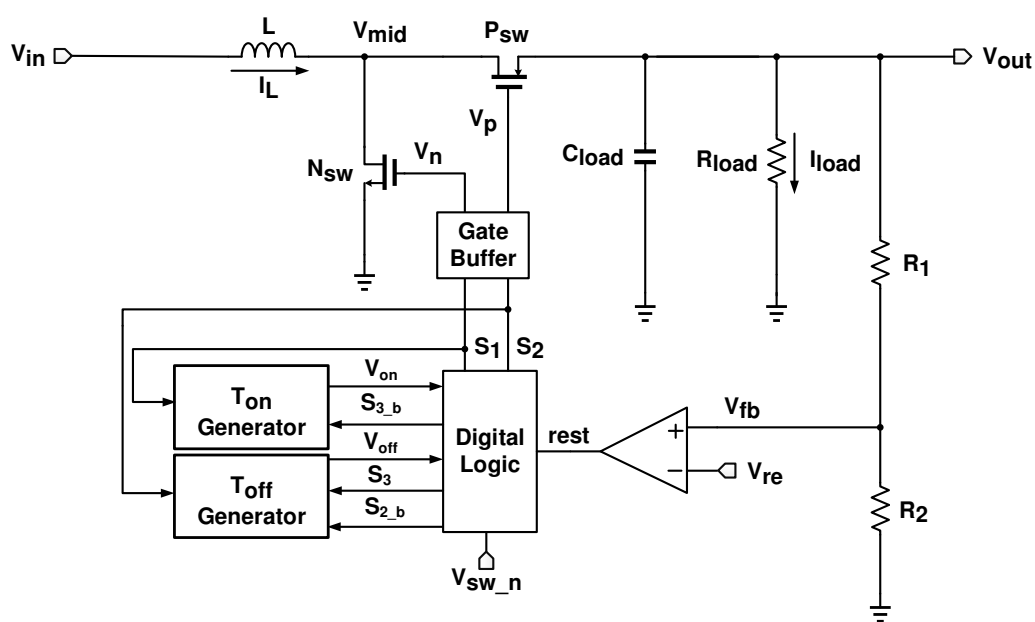


Figure 5. Boost DC/DC converter.

2.3.1. T_{on} Generator

The T_{on} Generator in Figure 5 is shown in Figure 6. It directs the V_n signal in Figure 5 to maintain the high pulse width ($V_n = 1$) which governs the ON time of the POWER NMOS N_{sw} . During T_{on} mode, S_1 is high, S_2 and S_3 are low, MN3 is turned on while MP4 is at cutoff. A fixed current (I_{on}) discharges C_{on} when $V_{con} < V_{in}$ is achieved. During T_{off} mode, S_1 and S_3 are low, S_2 is high, and MN3 and MP4 are at cutoff prior to becoming equal values of V_{con} and V_{in} . Figure 7 shows the timing diagram at T_{on} mode.

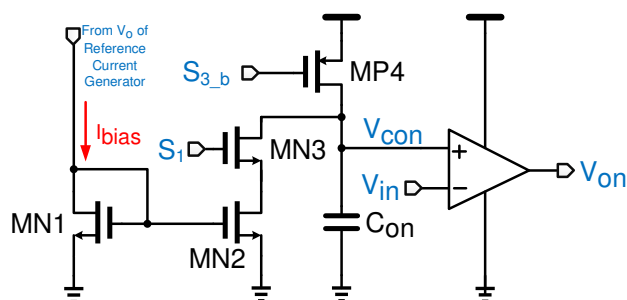


Figure 6. T_{on} generator.

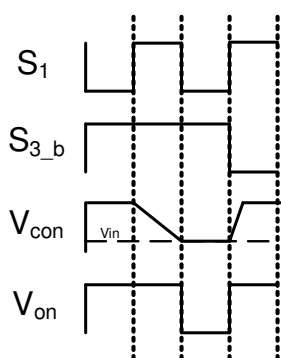


Figure 7. Timing diagram at T_{on} mode.

2.3.2. T_{off} Generator

The T_{off} generator in Figure 5 is shown in Figure 8. It directs the V_p signal to maintain the low pulse width ($V_p = 1$) for the ON time of power PMOS transistor P_{sw} , and generates charging and discharging currents through the current mirror. During T_{on} mode where S_1 is high, S_2 and S_3 are low, transistors MN7, MP10, and MN11 are at cutoff. On the contrary, during T_{off} mode, where S_1 and S_3 are low, S_2 is high, MN11 is at cutoff while MN7 and MP10 are on. Therefore, this charges C_{off} with a fixed current until $V_{coff} > V_{in}$ is expected. Figure 9 shows the timing diagram at T_{off} mode.

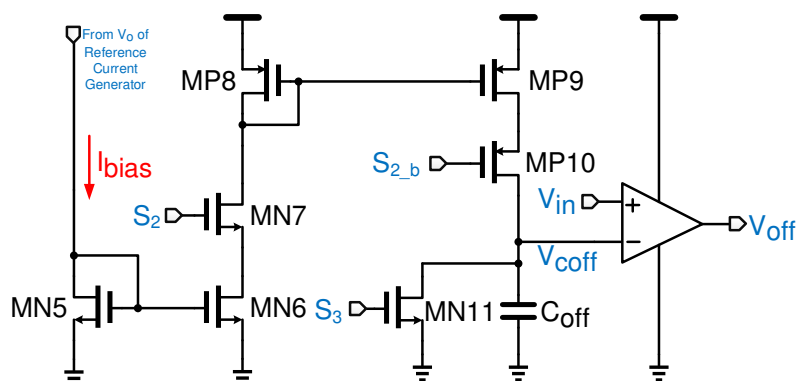


Figure 8. T_{off} generator.

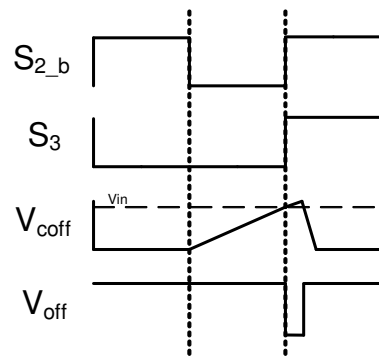


Figure 9. Timing diagram at T_{off} mode.

2.3.3. Digital Logic

Digital Logic in Figure 5 controls the signals' timing sequence in the DC/DC converter, so that the DC/DC converter follows a predefined function for it to be operated correctly.

Figures 10 and 11 show the flowchart and the timing diagram, respectively, of the timing control of Digital Logic in steady state. There are 3 modes: idle, on-time (T_{on}), and off-time (T_{off}). Looking at Figures 5 and 10, the DC/DC converter starts at idle mode, and Digital Logic is at initial state when V_{sw_n} is low and S_3 and V_{con} are high.

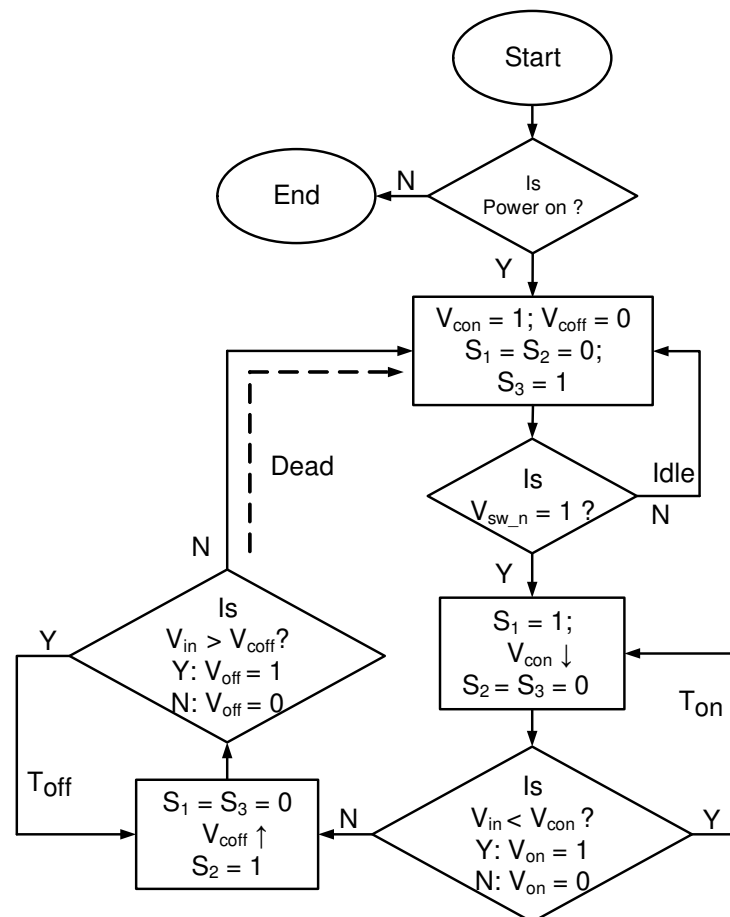


Figure 10. Flowchart of the timing control of Digital Logic.

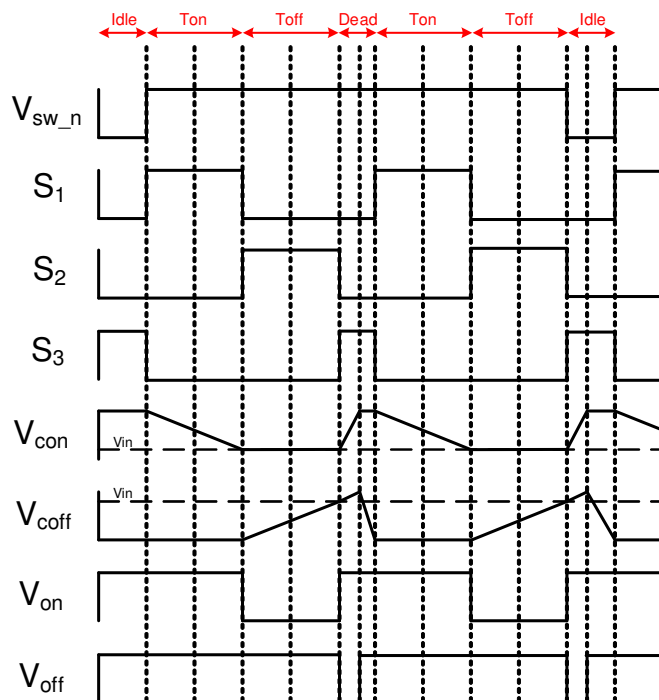


Figure 11. Timing diagram of the timing control of Digital Logic.

The power MOS transistor (M_{sw}) in Figure 2 will be on when a sufficiently high voltage is across C_{st} ; thus, making V_{sw_n} high. When S_1 which is connected to the Gate Buffer of N_{sw} and V_{sw_n} are high, and S_2 which is connected to the Gate Buffer of P_{sw} is low, the system enters T_{on} mode. At this time, the inductor L stores energy when I_L flows through N_{sw} . The T_{on} generator controls the duration of the T_{on} mode. It will enable S_1 to low after a predefined time when V_{con} drops below V_{in} changing the system from T_{on} to T_{off} mode.

When S_2 is high and S_1 is low, the system enters T_{off} mode. C_{load} charges when (I_L) flows through P_{sw} . The T_{off} generator controls the duration of the T_{off} mode. It will enable S_2 to low and S_3 to high after a predefined time when V_{in} drops below V_{coff} returning the system back from T_{off} to idle mode.

2.3.4. Reference Current Generator

Figure 12 shows the Reference Current Generator which provides a stable reference current (I_{bias}) needed in Figures 6 and 8. The duty cycle contributed by the power switches (N_{sw} and P_{sw}) depend on the Reference Current Generator. Since I_{bias} can be affected by power supply's voltage and temperature variations, proportional (PTAT) and complementary to absolute temperature (CTAT) circuits are implemented to suppress the influence of temperature on accuracy and stability. In PTAT, both MN1 and MN2 are driven to sub-threshold operation while both MP3 and MP4 are biased into strong inversion operation. PTAT current generator consists of transistors MN1, MN2, MP3, and MP4. Its generated I_{pt0} is mirrored by MP3 and MP9 to the resulting (I_{pt}). Moreover, CTAT current generator is composed of MP5, MN6, MN7, and MP8. Its I_{nt0} is mirrored by MP8 and MP9 to the output (I_{nt}). Then, the output current I_{bias} is the sum of I_{nt} and I_{pt} , which will be insensitive to temperature variations.

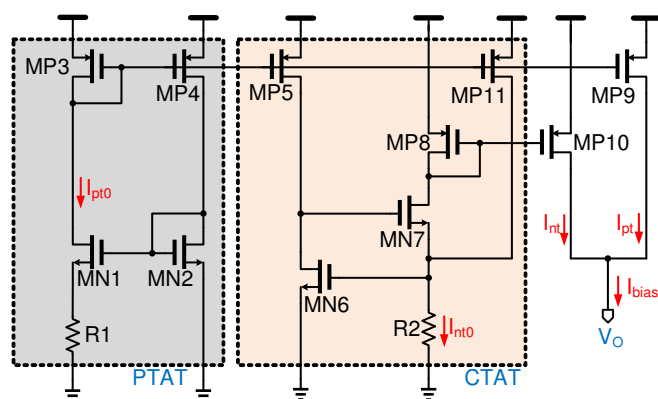


Figure 12. Reference current generator

2.3.5. Comparator Circuit

The two comparators in the T_{on} and T_{off} Generators are used to regulate the on-time and off-time modes’ maintenance duration, respectively. For these two comparators, their propagation delay and noise have less effect to the their function and performance than the output-regulated Comparator in Figure 5. Therefore, the two comparators’ quiescent current can be fixed to a smaller value to consume less power. However, the trade-off is that the propagation delay will be larger. In this design, a two-stage open-loop comparator is used for the AC/DC converter’s output adjustment. It is shown in Figure 13.

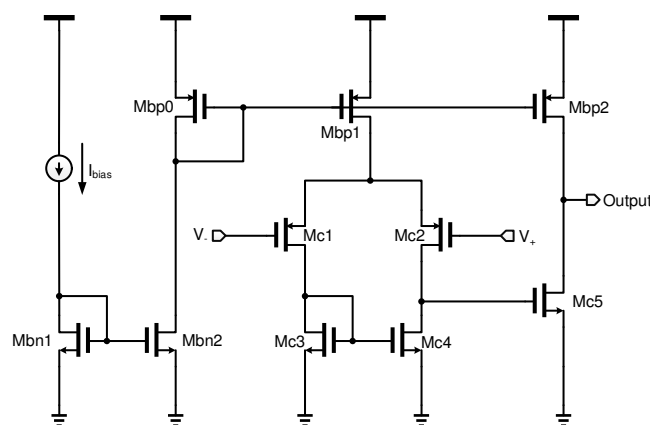


Figure 13. Comparator schematic

3. Measurement Results and Discussion

TSMC 40-nm CMOS process was used to implement and fabricate the PVDF piezo-electric energy harvesting IC. All of the transistor lengths are at minimum size. The aspect ratio of the width of the NMOS and PMOS transistors used in this chip is 2:1. The layout view of the core which has an area of $0.1223 \times 0.1065 \text{ mm}^2$ is shown in Figures 14 and 15 and shows the die photo of the chip which has an area of $0.7097 \times 0.7097 \text{ mm}^2$. The core was covered by a dummy layer, as seen in the die photo, because there is a minimum metal density required by the foundry; hence, only the pads and the wire-bonds can be seen in the photo.

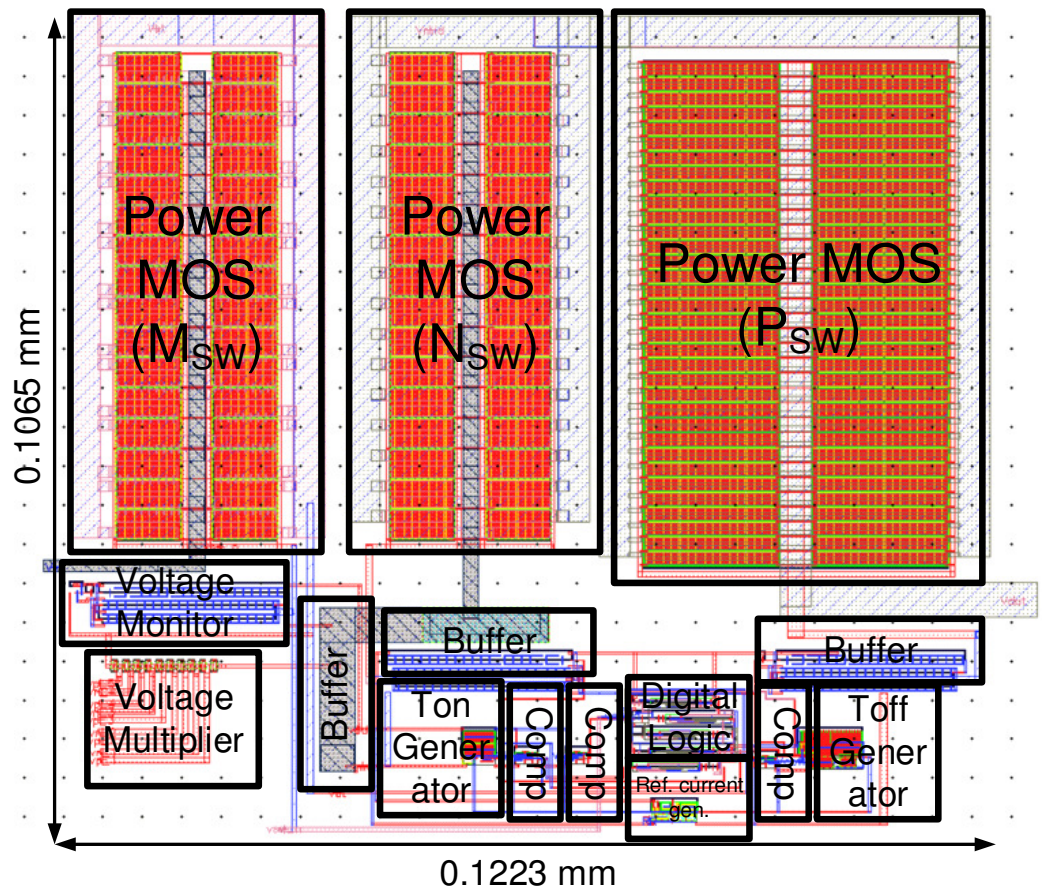


Figure 14. Core layout view of the piezoelectric energy harvesting IC.

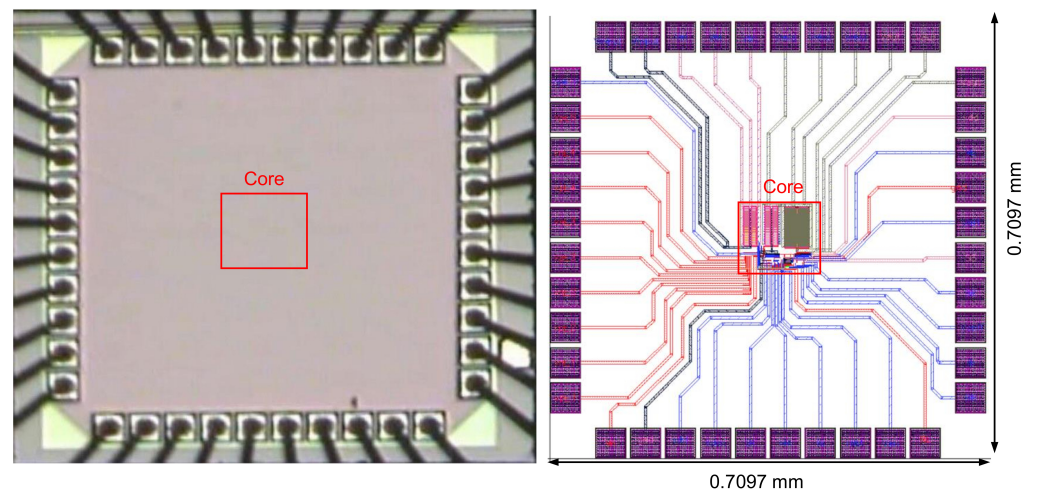


Figure 15. Die photo of the piezoelectric energy harvesting IC.

The fabricated chip was connected to PCB board and SMA connectors to reduce the loading effect. A power supply (ABM PRT3230 (ABM, Hsinchu City, Taiwan)) was used to provide VDD (0.9 V) and GND. A signal generator (Tektronix AFG3252 (Tektronix, Johnston, OH, USA)) provides input signals for testing. It generates a 120 mV-amplitude sinusoid which mimics the excitation and the output voltage of the PVDF film for easy testing and validation of the proposed energy harvesting circuit. An oscilloscope (Teledyne Lecroy Waverunner 610Zi (Teledyne Lecroy, Thousand Oaks, CA, USA)) observed the input

and output waveforms. It was also used for the measurement and characterization of the PVDF film's output voltage.

The output signal generated by the PVDF film, V_{st} , and V_{sw_n} signals are shown in Figure 16. A maximum of 100 kHz was used as PVDF's vibration frequency for this testing. From Figure 17, it is noted that at the beginning the capacitor (C_{st}) was charged at 260 mV. When V_{st} reaches at least 260 mV, the Voltage Monitor sends an enable signal ($V_{sw_n} = 1$ V) to the DC/DC Converter to start the second mode of boosting which is the T_{on} mode.

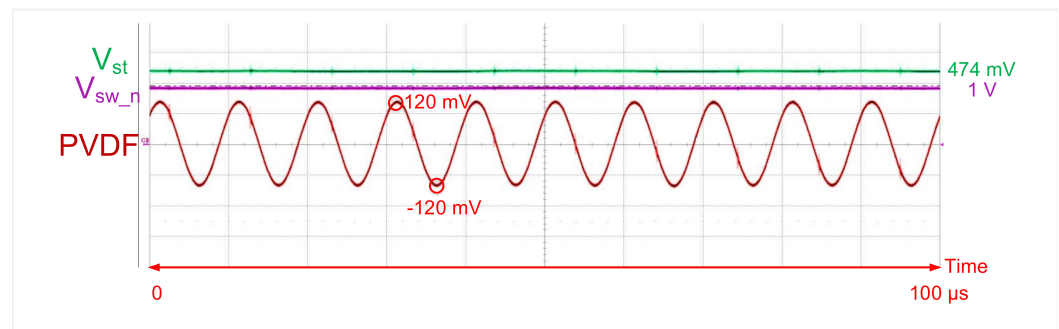


Figure 16. Waveforms of PVDF output signal, V_{st} , and V_{sw_n} .

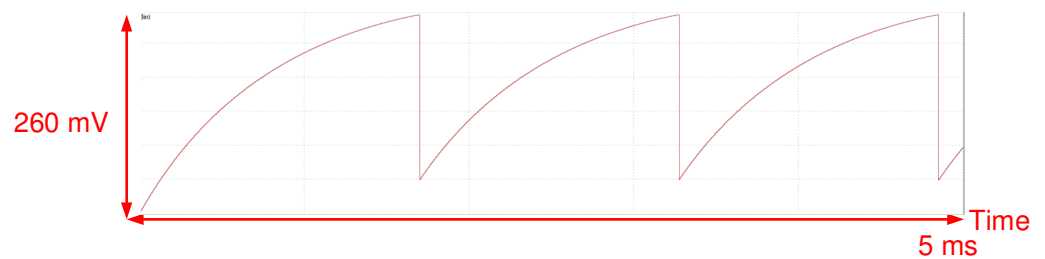


Figure 17. Waveform of the charging of capacitor C_{st} .

Figure 18 summarizes the output specifications. The output voltage, current, and power are 1 V, 4.2 mA, and 4.2 mW, respectively. When the on-voltage value (V_{on}) is lower than V_{st} (237 mV), V_{sw_n} is 0 then wait for the next enable signal. The resulting waveforms of the digital logic control in steady state is shown in Figure 18. It is consistent with the designed Digital Logic's timing control waveforms in Figure 19.



Figure 18. Waveforms of V_{out} , I_{load} , V_{st} , and V_{sw_n} .

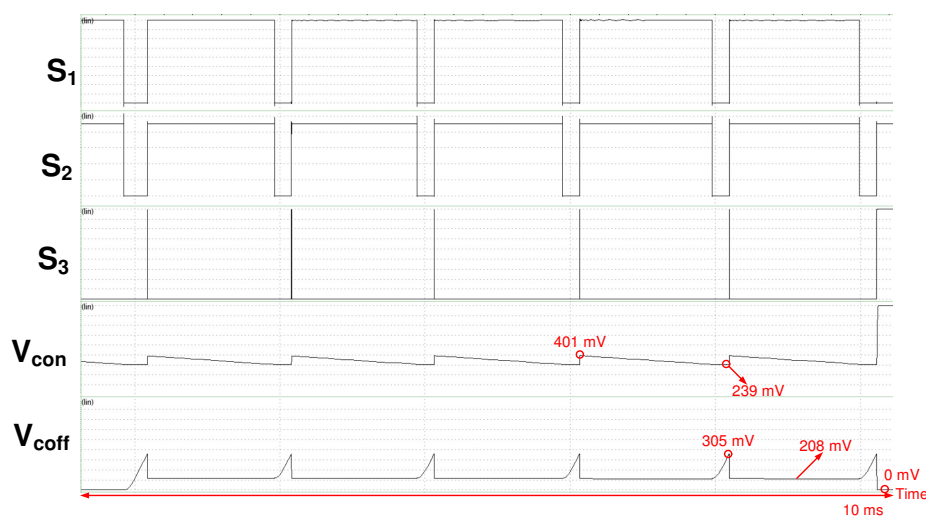


Figure 19. Digital Logic’s timing control waveforms.

Figure 20 shows the waveform of the output voltage V_{out} generated by the piezoelectric energy harvesting IC which is 1 V. For the PVDF generated voltage of 120 mV to 1 V, a regulated output voltage of 1 V is expected. The developed piezoelectric energy harvesting IC can be operated with a PVDF’s vibration frequency of 6.67 Hz to 100 kHz. The measurement results correspond with the post-layout simulation results made in the prior work [3]. With this, it can provide a stable power supply to the low-power and low-voltage wearable biomedical devices. The proposed piezoelectric energy harvesting IC is compared with the prior studies as shown in Table 1. In Table 1, it should be noted that the pump gain is represented as the ratio of V_{out} and the PVDF generated voltage. As shown in Table 1, the largest pump gain was generated by the proposed piezoelectric energy harvester IC over all the prior energy harvesting circuits cited in the literature.

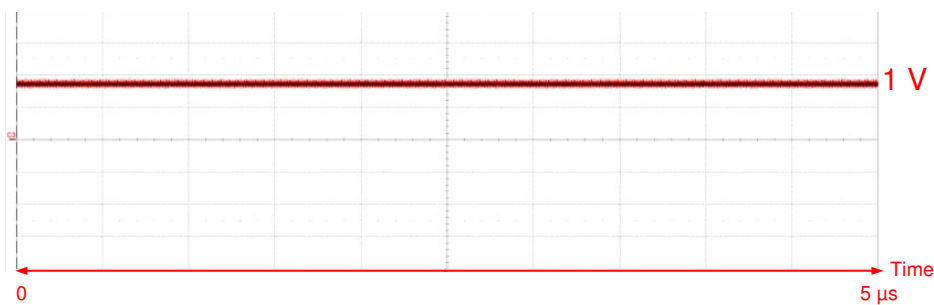


Figure 20. Waveform of V_{out} .

Table 1. Comparison of the piezoelectric energy harvesting circuit with prior studies.

	[13]	[8]	[14]	[15]	[16]	[17]	This work
Year	2017	2017	2017	2016	2014	2011	2021
Type	PZT	Vibrational	PVDF	Piezoelectric	PZT	Vibrational	PVDF
Process	0.5 μm	130 nm	130 nm	PSpice	0.18 μm	0.5 μm	40 nm
PVDF voltage	0.51 V	0.704 V	0.703 V	0.54 V	1 V	1 V	0.12 V
V_{out}	3 V	0.694 V	0.694 V	3.3 V	1.8 V	3 V	1 V
P_{out}	N.A.	10.7 μW	11.1 μW	57 mW	55 μW	3.9 mW	4.2 mW
Ripple	40 mV	N.A.	N.A.	N.A.	N.A.	N.A.	3 mV
Pump gain	5.88	0.987	0.987	6.11	1.80	3	8.33

4. Conclusions

A 40-nm CMOS piezoelectric energy harvesting IC has been presented. A Voltage Multiplier was constructed alleviating the problem of very low input voltage from the PVDF piezoelectric by boosting this low voltage. DC/DC converter improves the boosted voltage by following the Digital Logic's predefined timing of three operating modes, namely, idle, T_{on} , and T_{off} . With this, the low-power, low-voltage wearable biomedical devices, which normally require 1 V as their supply, can be operated at stable condition by the developed piezoelectric energy harvesting IC. Among the prior studies, the proposed energy harvesting IC exhibited the highest pump gain and accommodated the lowest piezoelectric generated voltage.

Author Contributions: Conceptualization, C.-C.W., L.K.S.T., P.-C.C., and J.R.E.H.; methodology, C.-C.W., L.K.S.T., P.-C.C., C.-K.Y., C.-T.P., and Y.-H.H.; software, P.-C.C.; validation, L.K.S.T. and P.-C.C.; formal analysis, L.K.S.T. and P.-C.C.; investigation, L.K.S.T. and P.-C.C.; resources, C.-C.W., C.-K.Y., and C.-T. P.; data curation, L.K.S.T. and P.-C.C.; writing—original draft preparation, C.-C.W., L.K.S.T., and P.-C.C.; writing—review and editing, C.-C.W., L.K.S.T., J.R.E.H., and Y.-H.H.; visualization, P.-C.C.; supervision, C.-C.W.; project administration, C.-C.W.; funding acquisition, C.-C.W. All authors have read and agreed to the published version of the manuscript.

Funding: This research was funded by Ministry of Science and Technology (MOST), Taiwan, under grant MOST 109-2218-E-110-007- and 109-2224-E-110-001-.

Acknowledgments: The authors thank Taiwan Semiconductor Research Institute (TSRI) for the EDA tool assistance and chip fabrication.

Conflicts of Interest: The authors declare no conflict of interest.

References

- Mahmood, M.F.; Mohammed, S.L.; Gharghan, S.K. Free Battery-based Energy Harvesting Techniques for Medical Devices. *IOP Conf. Ser. Mater. Sci. Eng.* **2020**, *745*, 1–17. [[CrossRef](#)]
- Arojanam, G.; Manivannan, N.; Harrison, D. Review on wearable technology sensors used in consumer sport applications. *Sensors* **2019**, *19*, 1983. [[CrossRef](#)] [[PubMed](#)]
- Wang, C.-C.; Chen, P.-C.; Hsueh, Y.-H.; Pan, C.-T.; Yen, C.-K.; Lee, T.-J.; Hizon, J.R. A PVDF-film energy harvesting circuit using 40-nm CMOS process. In Proceedings of the 2020 2nd International Conference on Smart Power & Internet Energy Systems (SPIES), Bangkok, Thailand, 15–18 September 2020.
- Khalid, S.; Raouf, I.; Khan, A.; Kim, N.; Kim, H.S. A Review of Human-Powered Energy Harvesting for Smart Electronics: Recent Progress and Challenges. *Int. J. Precis. Eng. Manuf.-Green Technol.* **2019**, *6*, 821–851. [[CrossRef](#)]
- Iqbal, M.; Nauman, M.M.; Khan, F.U.; Abas, P.E.; Cheok, Q.; Iqbal, A.; Aissa, B. Multimodal Hybrid Piezoelectric-Electromagnetic Insole Energy Harvester Using PVDF Generators. *Electronics* **2020**, *9*, 635. [[CrossRef](#)]
- Jeong, S.Y.; Cho, J.Y.; Hong, S.D.; Hwang, W.; Jabbar, H.; Ahn, J.H.; Jhun, J.P.; Sung, T.H. Self-Powered Operational Amplifying System with a Bipolar Voltage Generator Using a Piezoelectric Energy Harvester. *Electronics* **2020**, *9*, 41. [[CrossRef](#)]
- Fernandez, E.O.; Gobres, E.R.; Thio-ac, A.C.; Jandumon, M.S.; Ong, C.L.G.; Perez, R.B.; Ramos, P.G. Design Optimization of Low Power Wind Belt Electric Generator using Piezoelectric Transducer. In Proceedings of the 2018 IEEE 10th International Conference on Humanoid, Nanotechnology, Information Technology, Communication and Control, Environment and Management (HNICEM), Baguio City, Philippines, 29 November–2 December 2018.
- Oh, T.; Islam, S.K.; Mahfouz, M.; To, G. A Low-Power CMOS Piezoelectric Transducer Based Energy Harvesting Circuit for Wearable Sensors for Medical Applications. *J. Low Power Electron. Appl.* **2017**, *7*, 33. [[CrossRef](#)]
- Zhao, J.; You, Z. A Shoe-Embedded Piezoelectric Energy Harvester for Wearable Sensors. *Sensors* **2014**, *14*, 12497–12510. [[CrossRef](#)] [[PubMed](#)]
- Cepenas, M.; Peng, B.; Andriukaitis, D.; Ravikumar, C.; Markevicius, V.; Dubauskiene, N.; Navikas, D.; Valinevicius, A.; Zilyys, M.; Merfeldas, A.; et al. Research of PVDF Energy Harvester Cantilever Parameters for Experimental Model Realization. *Electronics* **2020**, *9*, 2030. [[CrossRef](#)]
- Caliò, R.; Rongala, U.B.; Camboni, D.; Milazzo, M.; Stefanini, C.; De Petris, G.; Oddo, C.M. Piezoelectric Energy Harvesting Solutions. *Sensors* **2014**, *14*, 4755–4790. [[CrossRef](#)] [[PubMed](#)]
- Pillatsch, P.; Yeatman, E.M.; Holmes, A.S.; Wright, P.K. Wireless power transfer system for a human motion energy harvester. *Sens. Actuators A Phys.* **2016**, *244*, 77–85. [[CrossRef](#)]
- Fan, S.; Zheng, X.-Q.; Wei, R.; Pulskamp, J.S.; Rudy, R.; Polcawich, R.G.; Feng, P.X.-L. mm-scale and MEMS piezoelectric energy harvesters powering on-chip cmos temperature sensing for IoT applications. In Proceedings of the IEEE 2017 19th International Conference on Solid-State Sensors, Actuators and Microsystems (TRANSDUCERS), Kaohsiung, Taiwan, 18–22 June 2017.

14. Mahbub, I.; Oh, T.; Shamsir, S.; Islam, S.K.; Pullano, S.A.; Fiorillo, A.S. Design of a pyroelectric charge amplifier and a piezoelectric energy harvester for a novel non-invasive wearable and self-powered respiratory monitoring system. In Proceedings of the 2017 IEEE Region 10 Humanitarian Technology Conference (R10-HTC), Dhaka, Bangladesh, 21–23 December 2017.
15. Mostafa, M.G.; Motakabber, S.M.A.; Ibrahimy, M.I. Design and analysis of a buck-boost converter circuit for piezoelectric energy harvesting system. In Proceedings of the 2016 International Conference on Computer and Communication Engineering (ICCCCE), Kuala Lumpur, Malaysia, 26–27 July 2016.
16. Aktakka, E.E.; Najafi, K. A micro inertial energy harvesting platform with self-supplied power management circuit for autonomous wireless sensor nodes. *IEEE J. Solid State Circ.* **2014**, *49*, 2017–2029. [[CrossRef](#)]
17. Rao, Y.; Arnold, D.P. An input-powered vibrational energy harvesting interface circuit with zero standby power. *IEEE Trans. Power Electron.* **2011**, *26*, 3524–3533. [[CrossRef](#)]
18. Vatansever, D.; Hadimani, R.L.; Shah, T.; Siores, E. An investigation of energy harvesting from renewable sources with PVDF and PZT. *Smart Mater. Struct.* **2011**, *20*, 1–6. [[CrossRef](#)]
19. Weng, P.S.; Tang, H.Y.; Ku, P.C.; Lu, L.H. 50 mV-input batteryless boost converter for thermal energy harvesting. *IEEE J. Solid State Circ.* **2013**, *48*, 1031–1041. [[CrossRef](#)]
20. Baker, R.J. *CMOS: Circuit Design, Layout, and Simulation*, 4th ed.; John Wiley & Sons: Hoboken, NJ, USA, 2019; pp. 523–528.
21. Wang, J. Design of a Boost DC-DC Converter for Energy Harvesting Applications in 40 nm CMOS Process. Master's Thesis, Delft University of Technology, Delft, The Netherlands, 2014.
22. Teh, Y.K.; Mok, P.K. A piezoelectric energy harvesting interface circuit using one-shot pulse transformer boost converter based on water bucket fountain strategy. In Proceedings of the 2014 IEEE International Symposium on Circuits and Systems (ISCAS), Melbourne, Australia, 1–5 June 2014.