Microelectronics Journal 114 (2021) 105127

Contents lists available at ScienceDirect

Microelectronics Journal

journal homepage: www.elsevier.com/locate/mejo

0.7 % error rate 3A bidirectional current sensor using high voltage CMOS process

Chua-Chin Wang *, Pang-Yen Lou, Zong-You Hou, Hsiu-Chun Tsai

National Sun Yat-Sen University, Department of Electrical Engineering, 70 Lian-Hai Rd., Kaohsiung, Taiwan

ARTICLE INFO

Keywords:
High-voltage (HV)
Bidirectional sensing
Input voltage range
Current sensor
Sensing error

ABSTRACT

This investigation demonstrates a high-accuracy bidirectional high-voltage (HV) current sensor fabricated using CMOS technology. Besides Noise filter, Sense stage, and Controller, the proposed sensor is featured with a Switching Network composed of transmission gates, which is able to steer the direction of the current for bidirectional sensing. A digital feedback loop comprises Controller generating a pair of digital signals to Switching Network such that the direction of the current is detected real time. The area of the proposed sensor on silicon is $1173 \times 664\ \mu m^2$ fabricated by 0.5 μm high-voltage CMOS process. The sensing voltage error is 0.7% by physical measurements, where the input voltage range is 8–14 V, and the current sensing range is -3 – 3 A.

1. Introduction

In any power system, the bidirectional current detection is very important for safety [1]. Traditional current sensors are found very hard to detect the bidirectional current in real-time operations such that detecting the bidirectional large current with high accuracy attacts strong attention [2–5]. Many researchers have reported several current sensor designs to resolve this issue, e.g. Refs. [6–8], basically using a low-resistance resistor as a sensing resistor in series with the load and then detecting the voltage drop thereof. Although the low-resistance resistors means to improve efficiency and accuracy, the intrinsic resistance variation results in large input offset to amplifiers [9]. Besides, to the best of our survey, all of the existing current sensors are focused on the detection of only one current direction. That is, they are not able to detect the discharge and charge currents of a battery system in run time, unless two sensors are used simultaneously. To resolve all the mentioned problems, a bidirectional current sensor using the fully-differential amplifier (FDA) with digital auxiliary circuits is proposed in this investigation. More specifically, the proposed sensor is featured with a digital feedback loop, where the sensed output voltage is sampled and converted into digital codes to drive Switching Network composed of transmission gates such that the correct current direction can be detected. The Switching Network not only correctly selects the direction of the current, but also elevates the accuracy higher than our previous work in Ref. [10]. With the assistance of external micro-controller, a simple FSM (finite state machine) is realized to automatically proceed the current sensing for charge-discharge-charge cyclic operations. The design was realized on silicon prototype and justified by physical measurements to sense the voltage from 8 to 14 V, and current range from −3 A to 3 A. Most important of all is that only 0.7% error is found to prove the accuracy of the proposed design.

2. High-voltage bidirectional current sensor

The block diagram of the proposed HV bidirectional current sensor is shown in Fig. 1, including a current sensing resistor (R_{cs}), a Noise filter, a Switching Network, a Sense Stage, R_{out}, an external micro-controller (MC), and a Controller. Fig. 2 shows the schematic of the proposed HV bidirectional current sensor, where all the details will be given in following text.

2.1. Operation of the proposed HV bidirectional current sensing

A very small sensing voltage (V_{cs}) is generated by I_{cs} via R_{cs}, where R_{cs} is a small resistor, as shown in Fig. 1. Noise filter comprising 4 R_{Nf}s and a C_{Nf} rejects unwanted high-frequency noise. I_t acts like a low-pass filter with a 3-dB bandwidth defined in Eqn. (1).

$$f_{-3dB} = \frac{1}{2\pi \cdot R_{Nf} \cdot C_{Nf}} \quad (1)$$

* Corresponding author. Institute of Undersea Technology (IUT) of NSYSU, Taiwan.
E-mail addresses: ccwang@ee.nsysu.edu.tw (C.-C. Wang), lou0105cat@vlsi.ee.nsysu.edu.tw (P.-Y. Lou), blazesky@vlsi.ee.nsysu.edu.tw (Z.-Y. Hou), roytsai94@vlsi.ee.nsysu.edu.tw (H.-C. Tsai).

https://doi.org/10.1016/j.mejo.2021.105127
Received 7 October 2020; Received in revised form 21 April 2021; Accepted 21 May 2021
Available online 18 June 2021

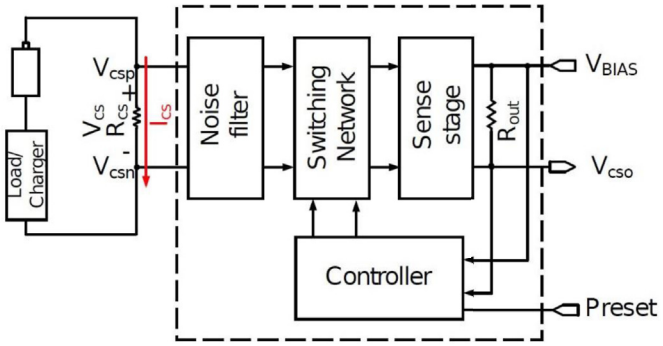

Fig. 1. Block diagram of the proposed HV current sensor.

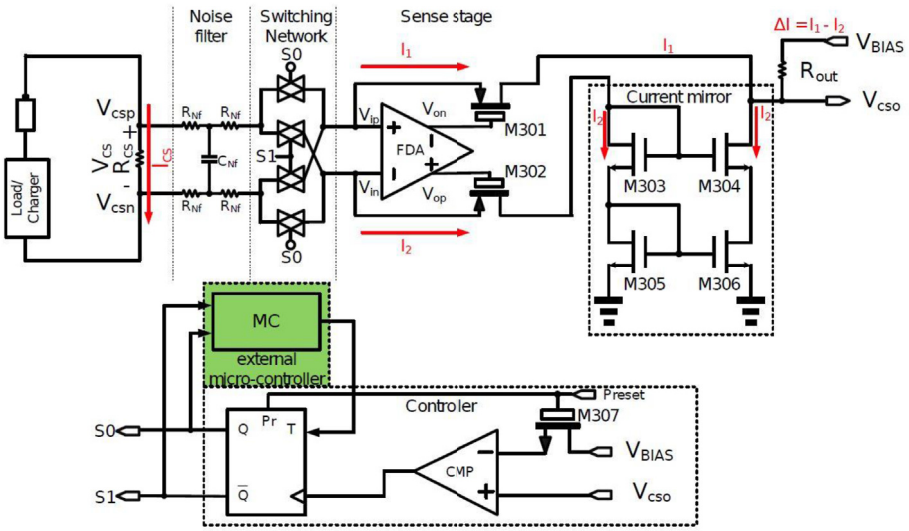

Fig. 2. Schematic of the proposed HV current sensor.

FDA in Sense Stage of Fig. 2 attains a virtual short across the input terminals (namely, $V_{ip} \cong V_{in}$) [10]. The drain currents of the M301 and M302 are then proportional to $(V_{csp}\text{-}V_{ip})/2R_{Nf}$ and $(V_{csn}\text{-}V_{ip})/2R_{Nf}$, respectively, assuming the transmission gates are ideal. Current mirror carries out the current subtraction to generate $\Delta I = I_1 - I_2$, whereupon ΔI is converted into an output voltage, V_{cso}, by R_{out}. The proposed sensing system's operations are classified into two modes:

- Discharge mode: When $V_{csp} > V_{csn}$ makes $I_1 > I_2$, the controller turns on S0, and then V_{BIAS} is kept higher than V_{cso} to inject current into the current mirror.
- Charge mode: When $V_{csp} < V_{csn}$ makes $I_1 < I_2$, the controller turns on S1, and then V_{BIAS} is lower than V_{cso}. The current would be steered away from V_{cso} to V_{BIAS}.

Assume the gain of the entire system is A_V. V_{cso} can be formulated as follows.

$$V_{cso} = V_{cs} \cdot A_V + V_{BIAS} \tag{2}$$

A_V can be written as follows:

$$A_V = \frac{R_{out}}{2 \cdot R_{Nf}} \tag{3}$$

Based on Eqns. (2) and (3), V_{cso} can be organized as follows:

$$V_{cso} = \frac{V_{cs} \cdot R_{out}}{2 \cdot R_{Nf}} + V_{BIAS} \tag{4}$$

Therefore, I_{cs} can be estimated indirectly using V_{cso}, as follows:

$$I_{cs} = \frac{V_{cs}}{R_{cs}} = \frac{(V_{cso} - V_{BIAS}) \cdot 2 \cdot R_{Nf}}{R_{out} \cdot R_{cs}} \tag{5}$$

2.2. FDA design

FDA in Fig. 2 is basically a two-stage fully-differential amplifier including a common-mode feedback, as shown in Fig. 3 [11]. Apparently, the common-mode voltage affects the output swing. Since the proposed sensor is meant to detect high voltage and current, which will easily generate significant common-mode offset. Thus, common-mode feedback circuit is needed, which regulates its common-mode voltage to a pre-defined value.

FDA shown in Fig. 3 is used to create virtual shorts and generate stable V_{op} and V_{on} to drive M301 and M302 into saturation, respectively. The saturation condition of PMOS is governed by Eqns. (6) and (7).

$$| V_{gs} - V_{th} | > 0 \tag{6}$$

$$| V_{ds} | > | V_{gs} - V_{th} | \tag{7}$$

where V_{th} is the PMOS threshold voltage. The common mode output voltage of FDA, namely V_{oc}, can be written as follows:

$$V_{oc} = \frac{V_{op} + V_{on}}{2} \tag{8}$$

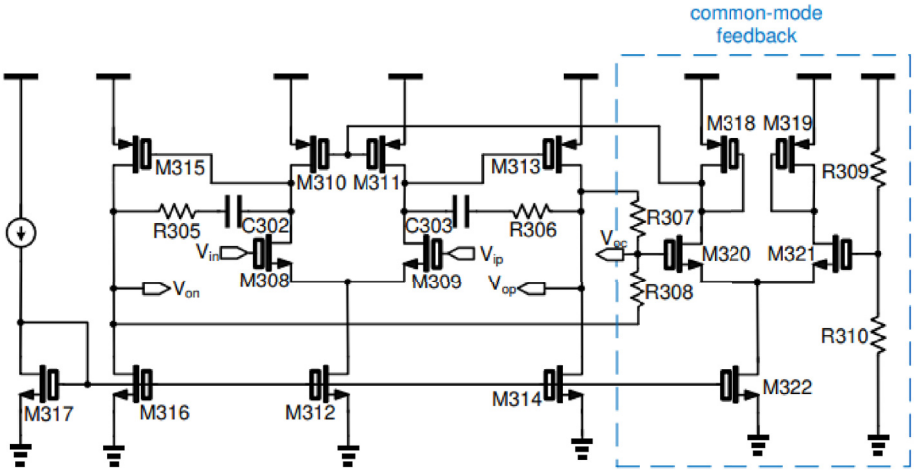

Fig. 3. Schematic of the proposed FDA [11].

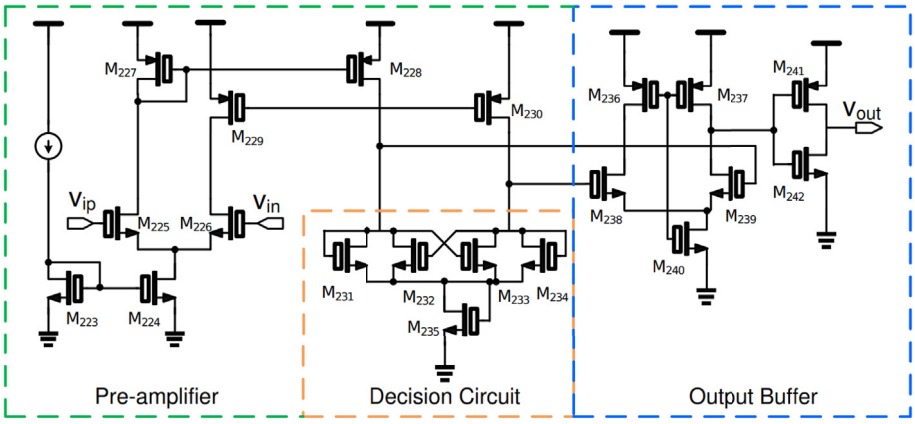

Fig. 4. Schematic of the proposed comparator.

Moreover, the differential mode output voltage of the FDA, namely V_{od}, is as follows [10]:

$$V_{od} = (V_{ip} - V_{in}) \times A_{FDA} \tag{9}$$

where A_{FDA} is the FDA gain. Thus, A_{FDA} can be summarized as follows:

$$A_{FDA} = gm_{M309}(r_{o,M309} \parallel r_{o,M311}) \cdot gm_{M313}(r_{o,M313} \parallel r_{o,M314}) \tag{10}$$

where $gm_{M313} = \mu C_{ox} \frac{W}{L}(V_{gs}\text{-}V_{th})$, $r_{o,M313}$ is the output resistance of M313, μ is the carrier mobility, and C_{ox} is the capacitance of the gate oxide. Based on Eqns. (8) and (9), the gate voltage of M301 ($V_{g,M301}$) and M302 ($V_{g,M302}$) can be derived as follows:

$$V_{g,M301} = V_{on} = V_{oc} + \frac{V_{od}}{2} \tag{11}$$

$$V_{g,M302} = V_{op} = V_{oc} - \frac{V_{od}}{2} \tag{12}$$

Thus, $V_{g,M301}$ and $V_{g,M302}$ can be re-organized as follows:

$$V_{g,M301} = \frac{V_{op} + V_{on}}{2} + \frac{(V_{ip} - V_{in}) \times A_{FDA}}{2} \tag{13}$$

$$V_{g,M302} = \frac{V_{op} + V_{on}}{2} - \frac{(V_{ip} - V_{in}) \times A_{FDA}}{2} \tag{14}$$

Thus, A_{FDA} should be tuned not too large to keep M301 and M302 saturated.

2.3. Controller design

Referring to Fig. 2 again, Controller comprises a comparator (CMP), a T flip-flop, and an external micro-controller (MC). Fig. 4 is the schematic of the proposed comparator. The operation is listed as follows.

(1). T flip-flop is activated by Preset. When Preset = 1, S0 = 1. Preset = 1 at power on and T = 1 in the initial state.
(2). CMP compares V_{cso} with V_{BIAS} to trigger T flip-flop. When V_{BIAS} is higher than V_{cso}, namely Discharge mode, S0 and S1 are kept unchanged. On the contrary, it will be in the Charge mode, and then T flip-flop pulls high S1, and S0 is pulled low.
(3). MC will generate T based on the previous state and the current state of the circuit as follows.
- The previous and the current states = Charge mode ⇒ T = 0.
- The previous state = Charge mode and the current state = Discharge mode ⇒ T = 1.
- The previous and the current states = Discharge mode ⇒ T = 0.
- The previous state = Discharge mode and the current state = Charge mode ⇒ T = 1.

(4). CMP compares V_{cso} with V_{BIAS} again to determine the states of S0 and S1.

This controller is in charge of the automatic bidirectional current sensing for the battery system no matter what the state is, either changed from discharge to charge, or vice versa. Fig. 5 is the flow chart of the controller. Preset is basically an enable signal to activate S0 and

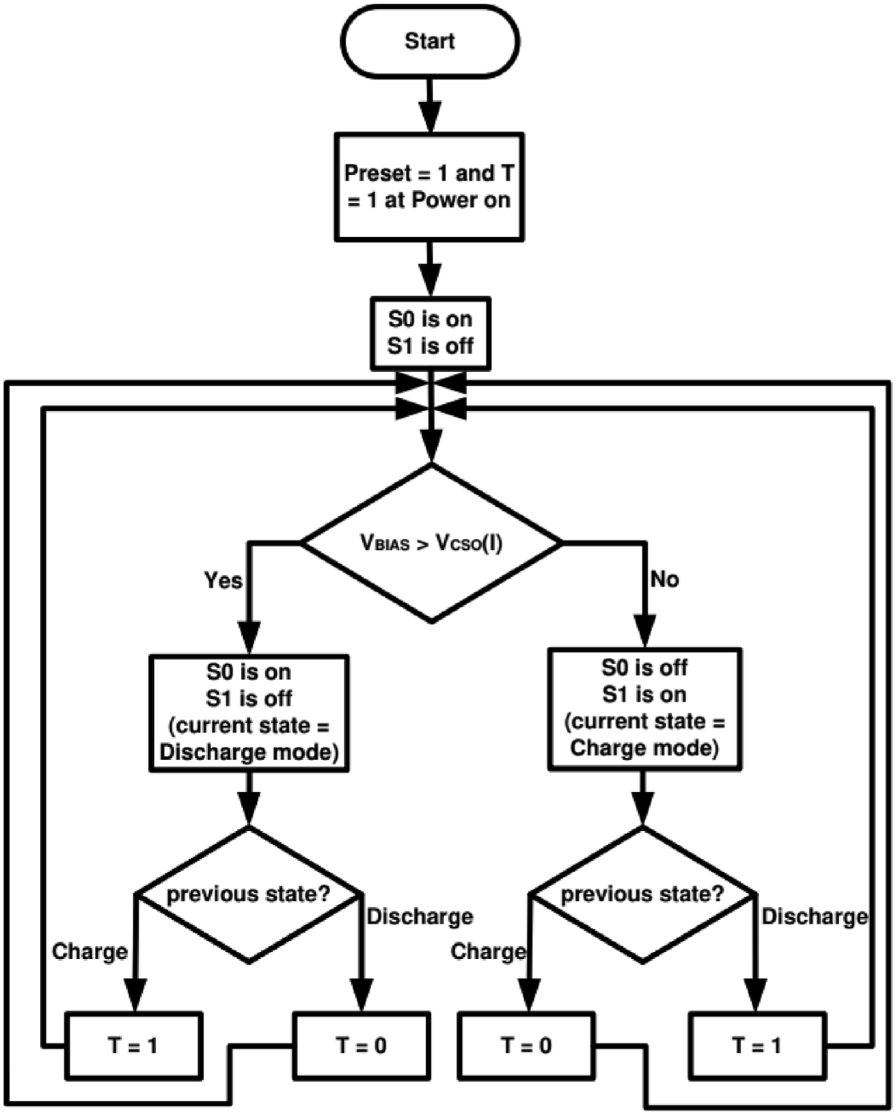

Fig. 5. The control flow of controller.

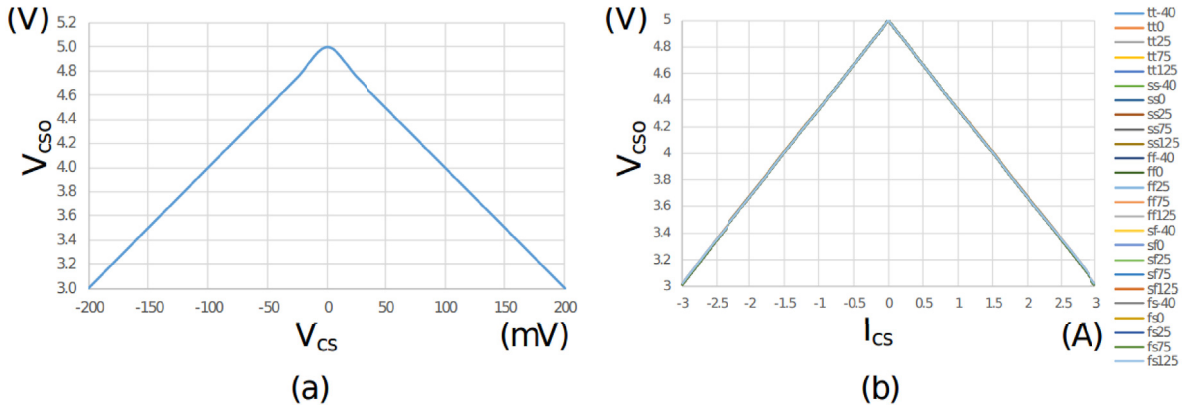

Fig. 6. All-PVT-corner simulations: (a) V_{cs} vs. V_{cso}; (b) I_{cs} vs. V_{cso}.

S1. When Preset becomes 1, S0 is high. Then, the Preset, S1, and S0 will change depending on the magnitudes of V_{BIAS} and $V_{caso}(I)$. Thus, controller can work correctly when the current direction changes at will.

3. Implementation and measurement

The proposed current sensor was fabricated using TSMC 0.5 μm CMOS high-voltage mixed-signal based LDMOS USG AL 2P3M polycide (T50UHV).

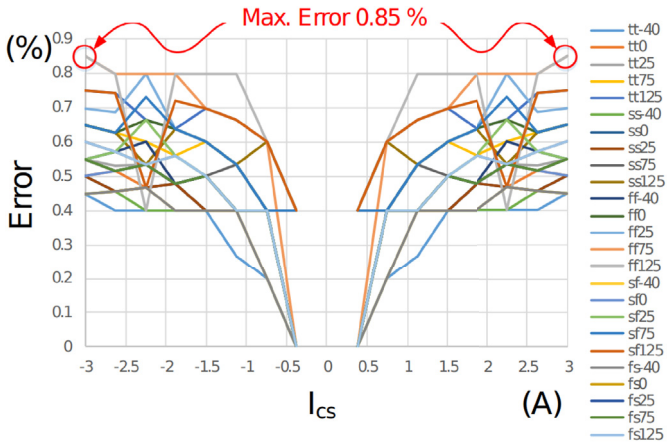

Fig. 7. Sensing voltage error distribution.

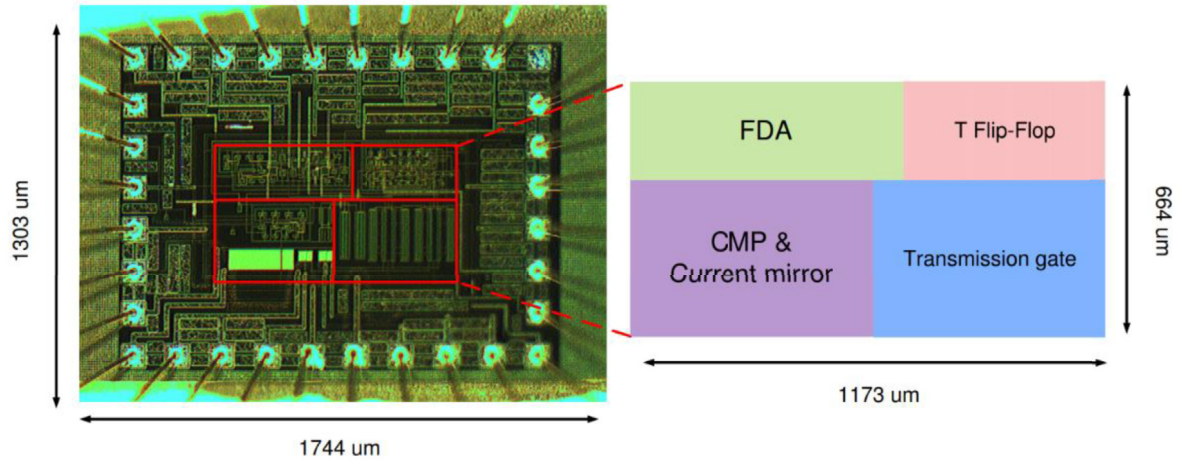

Fig. 8. Die photo of the proposed HV current sensor.

3.1. Post-layout simulations

To reject the high-frequency noise higher than 1.5 MHz, R_{Nf} = 10 kΩ, and C_{Nf} = 20 pF are used in the Noise filter (referring to Eqn. (1)). To enlarge the range of the sensor current, the smallest R_{cs} is selected to be 0.067 Ω in our design. Referring to Eqn. (2), a linear function is expected between V_{cso} and V_{cs}. Fig. 6 (a) shows post-layout simulations between V_{cs} and V_{cso} to verify this feature, when the sensed voltage (V_{cs}) range is -200 – 200 mV, and V_{BIAS} is 5 V. Moreover, Fig. 6 (b) is the all-PVT-corner (process, voltage, temperature) post-layout simulations of the proposed current sensor to validate Eqn. (5). It shows that when the sensing current range is -3 – 3 A, the output voltage range V_{cso} is 3–5 V. The proposed HV current sensor shows the worst-case sensing error of 0.85% when I_{cs} equals to ±3 A, as shown in Fig. 7. Besides, the average error is 0.48%.

3.2. Chip implementation and measurement setup

Fig. 8 shows the die photo of the proposed HV current sensor, where the chip area is 1744 × 1303 μm^2, and the core area is 1173 × 664 μm^2. The measurement setup with the battery module is shown in Fig. 9. The ANR26650 battery module is the real battery device to be tested [12], where the current magnitude is adjusted via an electronic load (PRODIGT 3311D Electronic Load). The power supply (Chroma 3201P-600-8) is in charge of supplying the required bias voltages (V_{BIAS}). An oscilloscope (Teledyne LeCroy - WaveRunner 610Zi) is used to monitor V_{cso}. Battery test equipment (LANHE CT2001D) is also used to assess the performance of the proposed HV current sensor.

3.3. Field measurement

To prove the performance of the proposed sensor working in the range of 8–14 V, the power supply generates 7 voltages (8, 9, 10, 11, 12, 13, 14 V). Meanwhile, the electronic load consumes 13 different currents in the range of 0–3 A, as shown in Fig. 10. Fig. 11 summarizes the error distribution at the 7 sensed voltages given the same current. The worst measured error is less than 1.22%.

Besides the experiment using equipments as the above, we use a real battery module consisting of 4S3R ANRANR26650 cells of which specification is given in Table 1. A battery testing system (LANHE CT2001D) was used to charge/discharge the battery module. Three chips fabricated with the proposed HV current sensor were used to carry out a total of 225 times measurements as summarized in Fig. 12. The standard deviation in the measurement results is smaller than ±3σ, as shown in Fig. 13. Table 2 tabulates a performance comparison of the proposed design and several recent works. Notably, our design is the only one to work in the range of 8–14 V and 0–3 A with maximum error of only ≤0.7%. Assume the FOM (figure of merit) is defined in Eqn. (15). Our design attains the best FOM of all the works.

$$\text{FOM} = \frac{\text{Voltage Range} \times \text{Sensing Current Range}}{\text{Core area} \times \text{Max. Error}} \tag{15}$$

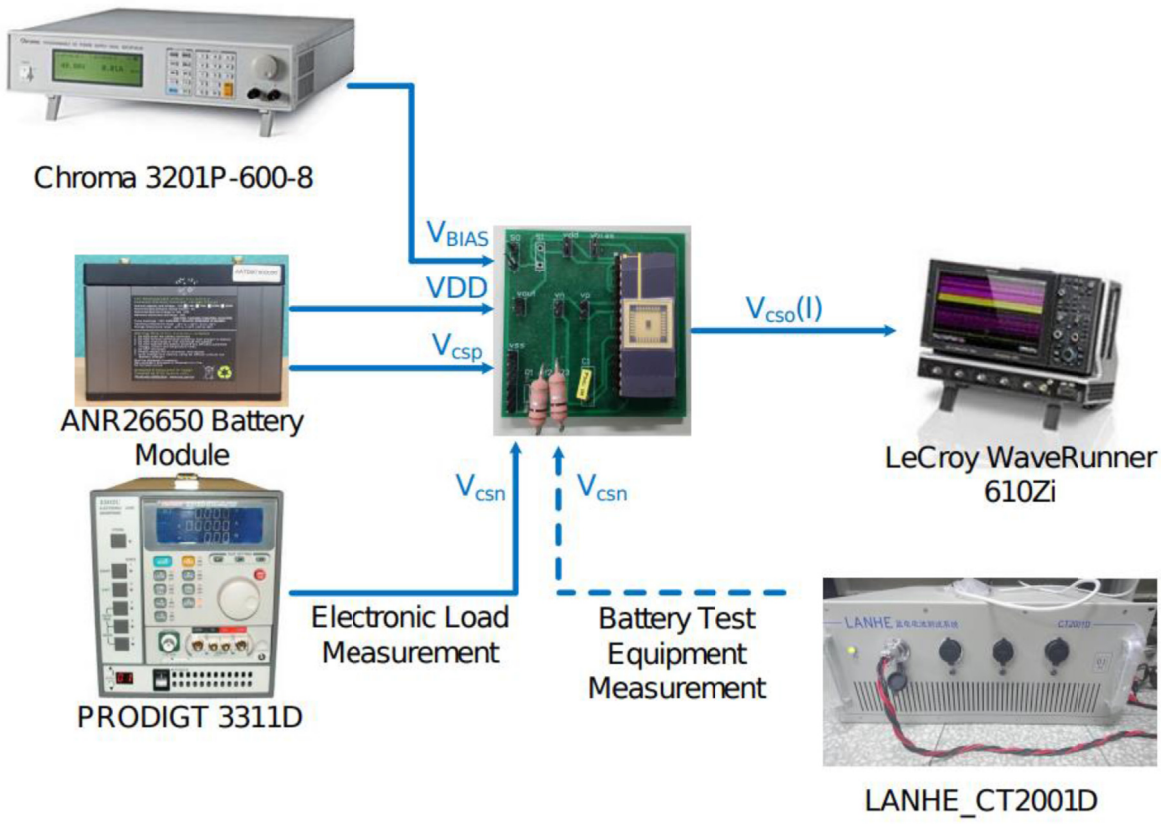

Fig. 9. Measurement setup of the proposed HV current sensor.

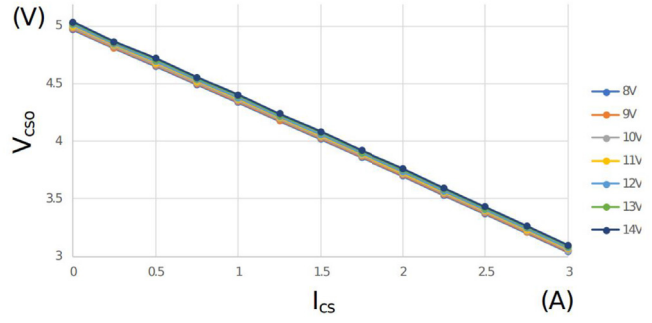

Fig. 10. Measurement results attained using the proposed HV current sensor.

Table 1
Cell specifications of the lithium-ion rechargeable battery (MODEL: ANR26650) [12].

	ANR26650
Nominal Voltage	3.3 V
Charge Voltage	3.6 V
Discharge Cutoff Voltage	2 V
Nominal Charge current	2.5 A
Maximum Charge current	10 A
Maximum Discharge current	50 A
Typical Capacity	2500 mAh
Minimum Capacity	2400 mAh

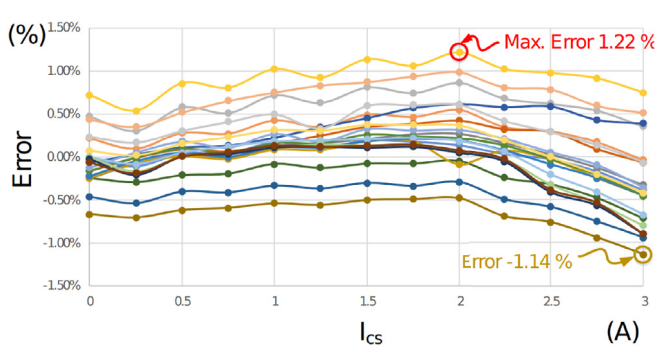

Fig. 11. V_{cso} error measurement attained using the proposed HV current sensor.

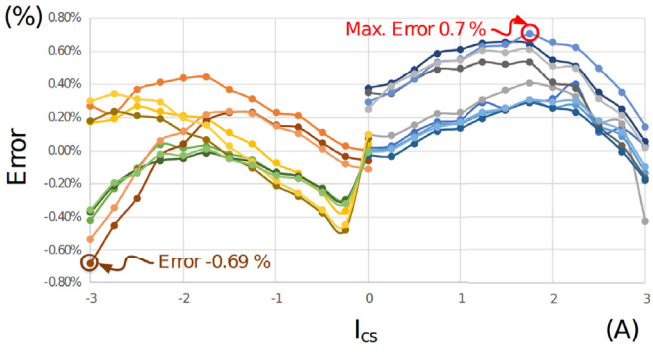

Fig. 12. V_{cso} error measurement in charge/discharge mode obtained using the proposed HV current sensor in real battery module testing.

Table 2
Comparison to state-of-the-art.

	[6] TPE	[7] TENCON	[8] INTELEC	[13] ICECS	[14] ISCAS	[15] LEM	This work
Year	2014	2015	2016	2016	2018	N/A	2020
Process	0.5 μm CMOS	0.25 μm BCD	PCB	0.18 μm HVCMOS	0.5 μm CMOS	Hall sensor	T50UHV CMOS
Implementation	Measurement	Measurement	Measurement	Simulation	Simulation	Measurement	Measurement
Bidirectional	No	No	No	No	No	No	Yes
Supply Voltage (V)	5.5	5	12	1.8 & 5	5	±15	5–20
Voltage Range (V)	2.7–4.5	36–55	1–12	36	5	±15	8–14
Sensing Current Range (A)	0.05–0.6	0.44–2.2	0–20	0.5–1.5	0–5	−3–3	**−3–3**
Max. Error (%)	4	2.5	3.3	1.2	3	±1.5	**0.7**($\leq \pm 3\sigma$)
Core Area (mm^2)	0.05	1.58	N/A	N/A	N/A	N/A	0.78
FOM	4.95	8.17	N/A	N/A	N/A	N/A	**76.923**

Note: σ: Standard deviation.

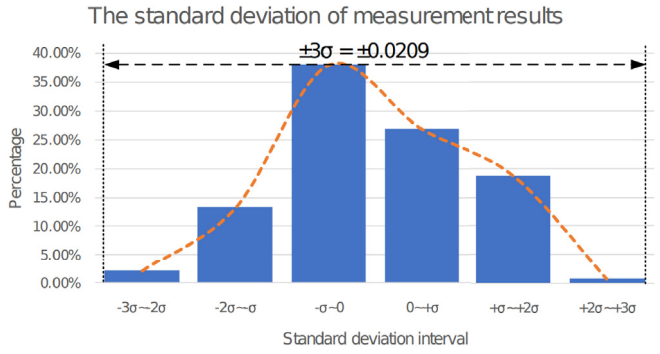

Fig. 13. Standard deviation of measurement results (225 times).

4. Conclusion

This investigation presents a high-accuracy CMOS HV bidirectional current sensor. Our design works in the input voltage range from 8 to 14 V. Moreover, it attains the very small sensing voltage error <0.7%. The design is featured with the digital feedback control to make bidirectional sensing feasible, and achieve the high accuracy at the same time.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Acknowledgment

This work was partially supported by Ministry of Science and Technology (MOST), Taiwan, under grant MOST 110-2218-E-110-008-, MOST 109-2241-E-110-001- and MOST 109-2218-E-110-007-. Moreover, this work was also partially supported by Ministry of Economic Affairs, Taiwan, under grant 107-EC-17-A-17-S3-050. The authors would like to express their deepest gratefulness to TSRI (Taiwan Semiconductor Research Institute), Taiwan, for their thoughtful chip fabrication service.

References

[1] T. Dong, J. Li, H. Dai, Analysis on the influence of measurement precision of the battery management system on the state of charge estimation, in: Proc. Asia-Pacific Power and Energy Engineering Conference (APPEEC), Mar. 2010, pp. 1–5.
[2] H.Q. Tay, V.T. Nam, N.H. Duc, B.N. Chau, A current sensing circuit using current-voltage conversion for PMOS-based LDO regulators, in: Proc. 2012 International Symposium on Computer Applications and Industrial Electronics (ISCAIE), Mar. 2012, pp. 1–4.
[3] F. Briffod, D. Alasia, L. Thevenaz, G. Cuenoud, P. Robert, Extreme current measurements using a fibre optics current sensor, in: Proc. 2002 15th Optical Fiber Sensors Conference Technical Digest., (OFS 2002), Aug. 2002, pp. 607–610.
[4] H. Zhou, C. Tan, J. Fletcher, Lossless bi-directional current sense circuit for low-voltage high-current DC/DC converters, in: Proc. IECON 2018 - 44th Annual Conference of the IEEE Industrial Electronics Society, Dec. 2018, pp. 1305–1308.
[5] Y. Wu, Y. Su, G. Han, Y. Wu, Q. Yi, G. Sun, D. Wang, Research on a novel bidirectional direct current circuit breaker, in: Proc. 2017 4th International Conference on Electric Power Equipment - Switching Technology (ICEPE-ST), Dec. 2017, pp. 370–374.
[6] H. Wang, X. Hu, Q. Liu, G. Zhao, D. Luo, An on-chip high-speed current sensor applied in the current-mode DC–DC converter, in: Proc. IEEE Transactions on Power Electronics (TPE), vol. 29, Sep. 2014, pp. 4479–4484. no. 9.
[7] W.-J. Lu, S.-S. Wang, M.-Y. Tseng, C.-C. Wang, A capacity monitoring system with HV current sensor and calibrated current estimation approach, in: Proc. IEEE Region 10 Conference (TENCON), Nov. 2015, pp. 1–4.
[8] K. Itoh, M. Muraguchi, T. Endoh, High accurate and low loss current sensing method with novel current path narrowing method for DC-DC converters and its demonstration, in: Proc. 2016 IEEE International Telecommunications Energy Conference (INTELEC), Oct. 2016, pp. 23–27.
[9] R. Channappanavar, S. Mishra, A novel bidirectional current estimator for digital controlled DC-DC converters, in: Proc. IEEE Applied Power Electronics Conference and Exposition (APEC), Mar. 2018, pp. 3068–3073.
[10] Z.-T. Hou, H.-C. Tasi, C.-C. Wang, High-voltage bidirectional current sensor, in: Proc. IEEE 12th International Conference on ASIC (ASICON), Oct. 2017, pp. 1145–1146.
[11] B. Razavi, Design of Analog CMOS Integrated Circuits, McGraw-Hill College, Aug. 2000, pp. 308–340.
[12] A123 SYSTEM, DataSheet: ANR26650m1-B, 2012.
[13] N. Mitrovic, R. Enne, H. Zimmermann, An integrated current sensing circuit with comparator function for a buck DC-DC converter in HV-CMOS, in: Proc. IEEE International Conference on Electronics, Circuits and Systems (ICECS), Dec. 2016, pp. 656–659.
[14] Y. Jiang, M. Swilam, S. Asar, A. Fayed, An accurate sense-FET-based inductor current sensor with wide sensing range for buck converters, in: Proc. IEEE International Symposium on Circuits and Systems (ISCAS), May 2018, pp. 1–4.
[15] LEM, LA 03-PB datasheet. [Online]. Internet: https://media.digikey.com/pdf/Data%20Sheets/LEM%20USA%20PDFs/LA%20PDFs/LA%2003%20.. %2020-PB.pdf.