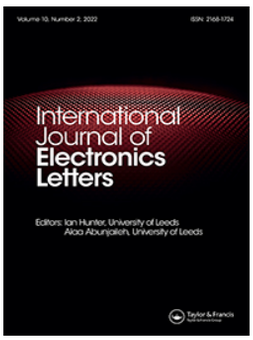

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A 100-MHz 3.352-mW 8-bit shift register using low-power DETFF using 90-nm CMOS process

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ABSTRACT

By keeping the very same transmission rate, a scheme is provided by DETFF (double-edge triggered flip-flops) for power dissipation reduction. As a result, they are suitable for use as shift registers. This investigation discussed various previous DETFF designs and demonstrated a new DETFF circuit applied to construct an 8-bit low-power shift register. This study makes a significant contribution by using two parallel data paths that operate in a single clock's opposing phases where an inverted input trigger is unnecessary. TSMC 90-nm complementary metal-oxide semiconductor (CMOS) technology was used to implement the proposed shift register. Comparing the proposed DETFF with prior works, it has fewer transistor counts since the negated input trigger and auxiliary devices were removed, resulting in lower area cost and lower power dissipation. At 100 MHz clock frequency and lower supply voltage of 1.0 V, it demonstrates a power consumption of 3.352 mW on silicon, making it suitable for low-power applications. Lastly, it has the best performance compared with prior works speaking of larger scale, as demonstrated by the chip's functionality and jitter measurement at the maximum frequency of 200 MHz.

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KEYWORDS
Double-edge triggered; CMOS; low power; dual path; measurement

1. Introduction

Flip-flops are fundamental sub-circuits of every digital system. Due to the sequential logic circuit's reliance on the current input and previous output, shift registers or flip-flops are needed to maintain the system's state (Wang et al., 2006, 2010). Additionally, a shift register can perform mathematical operations such as addition, data shifting, and multiplication. As a result, they are mainly employed to store and transfer digital data (Baskoro et al., 2018; Tolentino et al., 2018, 2019). The most challenging aspect of an IC designer's job is designing a digital chip that can perform at the highest throughput while still using little power, resulting in more conserved energy.

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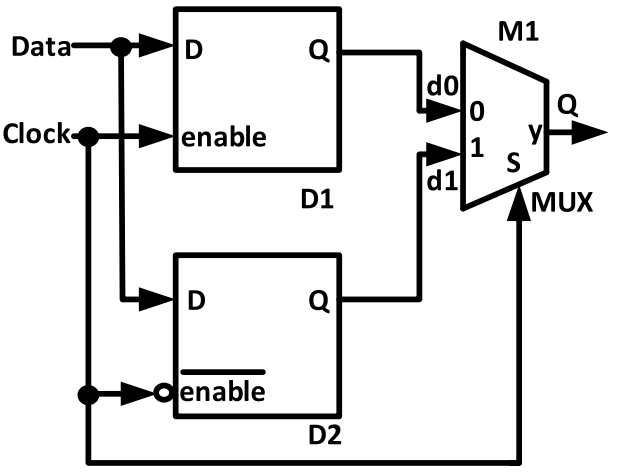

Figure 1. Typical DETFF circuit implementation (Baskoro et al., 2018).

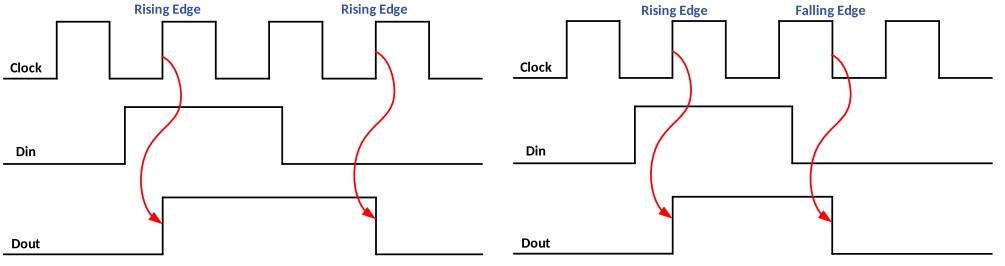

Figure 2. Difference between SETFF and DETFF based on functionality.

1.1. Double-Edge Triggered Flip-Flop (DETFF)

Figure 1 shows a typical double-edge triggered flip-flop (DETFF) circuit implementation, which comprises positive (D1) and negative (D2) level-sensitive latches (Baskoro et al., 2018). Moreover, a DETFF includes a multiplexer (M1) as denoted by Equation (1):

$$y = d_0(s') + d_1(s) \tag{1}$$

Additionally, a DETFF has the unusual property of latching data on either the rising or falling edge, which is anticipated to decrease power consumption with no adverse consequences substantially. At the same time, a single-edge triggered flip-flop (SETFF) cannot (Baskoro et al., 2018; Lang & Shen, 2013). Figure 2 shows the difference between SETFF and DETFF based on their functionality. Overall, by using DETFF, comparable data throughput can be retained by system designers at a slower clock frequency (Baskoro et al., 2018; Moisiadis et al., 2001; Sharma & Singh, 2016; Wang et al., 2010). As a result, implementing the DETFF in a high-resolution shift register is a prudent choice (Murugasami & Ragupathy, 2020).

1.2. Hypothesis and limitations of the developed methods presented by prior works

There are many methods for implementing a DETFF. First, an XOR gate with a delay circuit that generates internal pulse signals on every clock edge is implemented (Baskoro et al., 2018; Wang et al., 2010). Second, the path is repeated, allowing the flip-flop for data bit to be sampled on each edge of the clock (Yu & Tsai, 2018). Implementing double-edge triggering, also known as latching, minimises the overhead associated with sequencing, often utilised in pipelining systems (Wang et al., 2000, 1998).

Because built-in self-test (BIST), an essential requirement for testability, supports a wider variety of low-power applications, most digital systems utilise the BIST for internal testing. An 8-bit reversible linear phase shift register was developed by Kumar et al. (2017) that reduced the power consumption of the standard LFSR by 10%. An 8-bit LFSR with a weighted random test pattern generator was presented by Bagalkoti et al. (2019) to enhance overall performance, which results in a decrease in time delay but has a trade-off of higher power consumption. Meanwhile, a 256-bit shift register that uses bi-enabled pulse latches was developed by Authimuthu et al. (2022) to replace the commonly-used flip-flops. However, it is implemented using a legacy process (180 nm CMOS) and a higher supply voltage (1.8 V). Another shift register was designed by Jeon (2020) based on quantum-dot cellular automata (QCA) and electronic correlations. It demonstrated high efficiency regarding energy dissipation, time complexity, and optimised area & latency. Compared to using logical effort analysis, the power & area efficiencies and power-delay product (PDP) were optimised in two DETFFs using elephant herding optimisation (EHO) (Sabu & Batri, 2020a, 2020b) and interior search (ISA) & gravitational search (GSA) algorithms (Singh et al., 2018). However, these designs were only proven by simulation results (Jeon, 2020; Sabu & Batri, 2020a,b; Singh et al., 2018). Previously, we presented and designed an 8-bit shift register using DETFF (Ekkurthi et al., 2021). The proposed DETFF design underwent post-layout simulations only, so there was no theoretical analysis or chip measurement. For all of the above concerns to be addressed, a DETFF-based 8-bit shift register fabricated and tested on silicon is presented in this paper to minimise the delay and reduce the power consumption simultaneously.

2. System architecture of the DETFF Using 90-nm CMOS

2.1. DETFF of *Yu and Tsai (**2018**)*

A one-bit DETFF described by Yu and Tsai (2018) is illustrated in Figure 3, comprising an output keeper circuit, two latches, and six pass transistors. Inverters arranged in a back-to-back structure (I11 & I12 and I13 & I14) constitute the two latches. The whole arrangement seems complex. Also, based on the circuit's structure, it will take longer for output Q to reach, resulting in higher power consumption. The functionality was still the same when the output keeper circuit replaced the two latches.

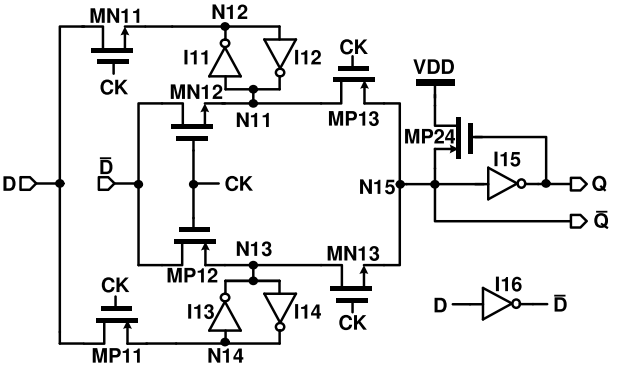

Figure 3. DETFF of Yu and Tsai (2018).

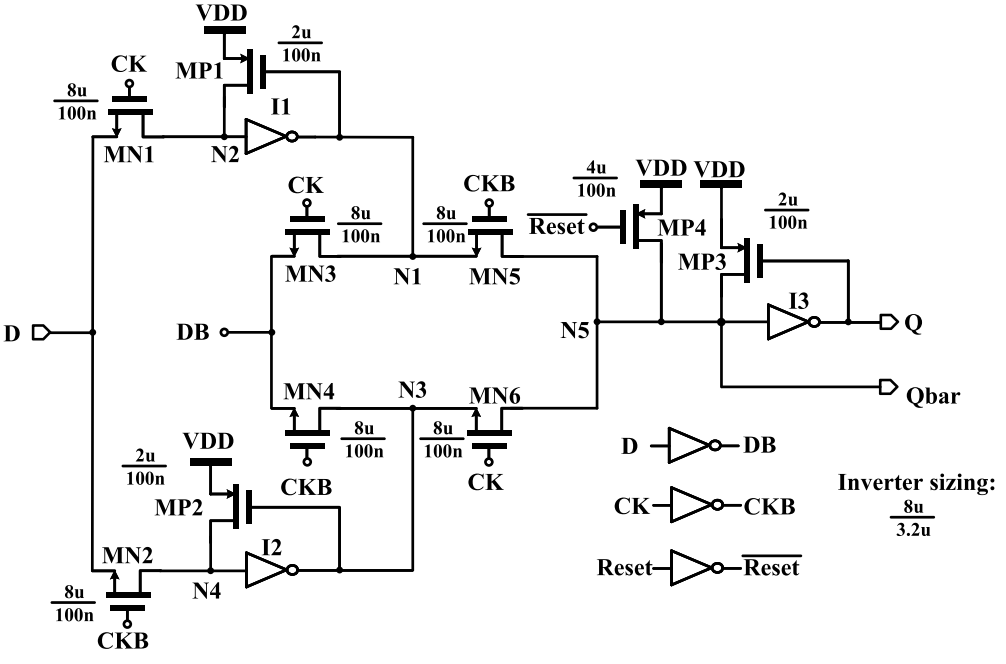

Figure 4. Traditional DETFF implemented in a 90-nm process based on prior work of Chu (2019).

2.2. DETFF of *Chu (2019)*

Meanwhile, a traditional DETFF proposed by Chu (2019) is shown in Figure 4. It consists of 6 N-type transistor switches (MN1, MN2, MN3, MN4, MN5, MN6), two latches, and an output keeper circuit. The register is composed of inverter I1 & P-type transistor MP1 and inverter I2 & P-type transistor MP2. The output keeper circuit comprises an inverter I3 and a feedback transistor MP3.

Faster transmission speed is one advantage of this DETFF. To solve the problem of the voltage loss across the NMOS device at logic 1, i.e. VDD – Vthn, a latch, and a PMOS transistor were used to form a keeper. Two inputs for each set of latches were implemented to solve the problem of the low full swing of NMOS switches. Each switching

transistor is controlled by a pair of the same clock control signal (CK) or inverted clock control signal (CKB). The input terminals of each group of input switching transistors use complementary input signals (D, DB). Even if the signal transmitted by one of the NMOS has a voltage of VDD – Vthn, the other NMOS that sends the complementary signal must transmit a low-level signal. Then, the node storing the VDD – Vthn potential is pulled high to VDD potential.

Moreover, the operation of this DETFF is stated as follows:

- CK: low to high.

When CK is low while CKB is high, transistors MN2, MN4, and MN5 are turned on, and MN1, MN3, and MN6 are off. Since MN2 and MN4 are on and MN6 is off, the input signal D passes through MN4 and inverter I2, and N3 is switched by the latch formed by inverter I2 and feedback transistor MP2. At the same time, because MN5 is turned on since CKB is high, the data signal on node N1 passes through MN5 and inverter I3 and then passes to output Q. The feedback transistor MP3 is turned on if the output Q is low. The node N5 voltage is pulled up to VDD.

- CK: high to low.

When CK is high while CKB is low, transistors MN1, MN3, and MN6 are turned on, and MN2, MN4, and MN5 are off. Since MN1 and MN3 are on and MN5 is off, D passes through MN1 and inverter I1, and N1 is switched by the latch inverter I1 and feedback transistor MP1. At the same time, because MN6 is turned on since CK is high, the data signal on node N3 passes through MN6 and inverter I3 and then passes to output Q.

- Reset:

When the Reset signal is high, MP4 is on, and node N5 will be pulled up to VDD. After passing through inverter I3, Q will be low.

2.3. Design considerations of low-power DETFF

By eliminating the negated input trigger and the subsequent devices, MN12 and MP12, the proposed DETFF architecture in Figure 5 is improved. The flip-flop's functionality is not only affected by these added devices. The transistor count is also reduced; thus, resulting in a lower area of the core, lower cost, and lower power dissipation.

The proposed work is improved by taking the following aspects into account:

- Looking into N23 node, the proposed work has 1 gate capacitance and 1 diffusion capacitance exhibited by devices MP21 and MN23, respectively. On the contrary, the said one-bit DETFF in Figure 3 has 2 gate capacitance and two diffusion capacitance exhibited by inverter I11 and devices, MN12 & MP13, respectively. Thus, node N23's load is smaller, resulting in a decrease in consumed power, charging period, and discharging period. The switching power (Psw) is directly related to the product of clock frequency (f), capacitance (C), and supply voltage (VDD) as shown in Equation. (2).

$$P_{sw} = f \cdot C \cdot V_{DD}^2 \tag{2}$$

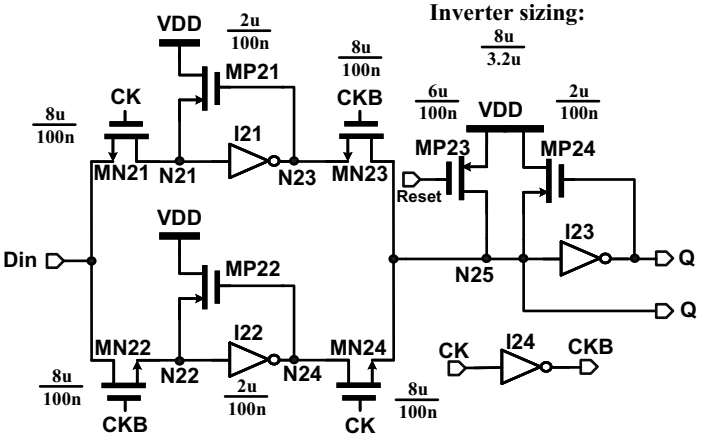

Figure 5. Proposed DETFF.

Suppose that both designs have same values for the frequency and supply voltage; the expressions for their power values at N11 and N23 nodes are directly proportional to gate capacitance (C_g) and diffusion capacitance (C_{diff}) as stated in Equation (3) and (4):

$$P_{N11} \propto 2C_g + 2C_{diff} \tag{3}$$

$$P_{N23} \propto C_g + C_{diff} \tag{4}$$

Using TSMC 0.18-μ m 1P6M CMOS process as an illustration, where C_g is 0.4 nF, and C_{diff} is 0.25 nF, P_{N23} is 0.5 times that of P_{N11}. During the inverse clock phase, the consumed power at N13 and N24 is the same throughout.

- N11 and N23's power consumption may be calculated using drain current (ID) and gate-source voltages (V_{gs}). ID is represented by Equation (5).

$$I_D = \frac{1}{2} \cdot \frac{W}{L} \cdot \mu_n \cdot C_{ox} \cdot (V_{gs} - V_{th})^2 \tag{5}$$

where W is the gate width, L is the gate length, μ_n is charge mobility, and V_{th} is the threshold voltage. Based on Equation (2) and (5), switching power consumption is directly related to ID. Thus, both V_{gs} and power increase as ID increases. Looking at Figure 3 and 5, these numerous devices contribute to higher V_{gs} at N11 than at N23. With this, a higher power is consumed at N11 than at N23. Similarly, the consumed power at N13 and N24 will be alike during the inverse clock phase.

- Due to the fact that this design in Figure 5 uses fewer devices than the design in Figure 3, the clock line routing is simplified, resulting in a reduction in clock power consumption.

As a result, these considerations imply that our DETFF has lower power consumption than previous efforts.

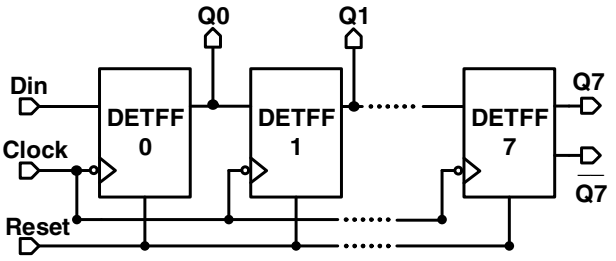

Figure 6. 8-bit DETFF-based shift register's block diagram.

2.4. Shift register based on new DETFF

As mentioned before, the proposed DETFF architecture utilises the dual path to allow the flip-flop for data sampling on each edge of the clock. The operation is as follows:

- CK = high: The switched-on transistors are MN21 and MN24, while switched-off transistors are MN22 and MN23 are turned off during the positive edge of the clock signal (CK). MN21 receives input signal Din, and I21 inverts this signal. N23 stores this inverted signal until CK is low.
- CK = low: CKB is now high, and MN23 is off. Hence, the N23's stored signal gives the output Q according to the reset. On the contrary, MN22 receives the input signal Din when CK is low.

A similar procedure as in the first path is repeated. If voltage swing is present and evident when several devices receive these signals, the signal should be boosted by utilising MP21, MP22, and MP24, which are regenerative transistors connected to VDD. Throughout the said continuous operation, Q is monitored at each clock edge. In short, upper and lower pathways' functions are interchanged during the opposite phase of CK. This demonstrates alternate sampling and transferring behaviour.

As shown in Figure 6, an 8-bit shift register utilised the proposed DETFF to prove the DETFF's functionality. Similar clock and the reset signals are used in the conventional shift register.

3. Measurement setup of the proposed DETFF

TSMC mixed-signal/RF 1P9M low-power 90-nm CMOS process with ultra-thick (34 kA) top metal options was used to fabricate the shift register. Figure 7 shows the schematic of the whole chip. For a fair comparison, a prior shift register shown in Figure 4 (Chu, 2019) was also realised with the proposed work on the same die. Meanwhile, Figure 8 illustrates the (a) die photo, (b) floor plan, and (c) layout of the whole chip. $966 \times 966\ \mu m^2$ is the area of the chip, while $215.8 \times 162.5\ \mu m^2$ is the active area. Figure 9 presents the core layout of the proposed 8-bit shift register.

Figure 10 shows the measurement setup of the proposed chip. Supply voltage is provided by Agilent N6761A. Agilent 81250 generated input signals, namely clock (CLK), multiplexer and demultiplexer's selection lines (S0 & S1), and data input (Din).

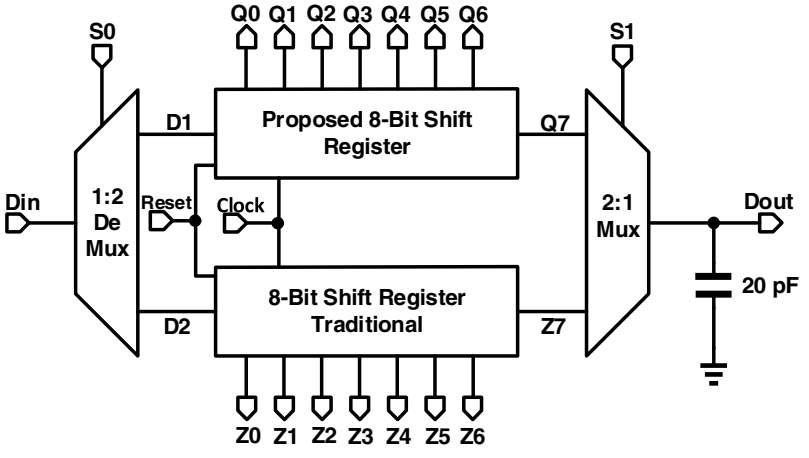

Figure 7. Proposed 8-bit DETFF-based shift register's schematic.

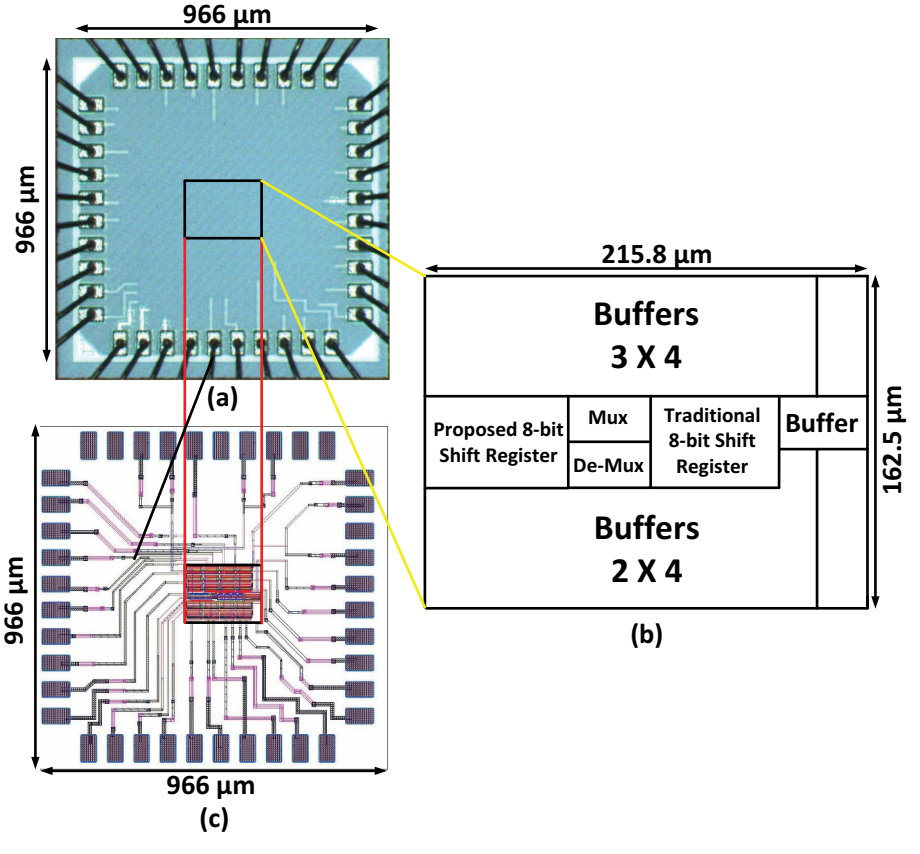

Figure 8. (a) Die photo, (b) floor plan, and (c) chip layout of 8-bit DETFF-based shift register.

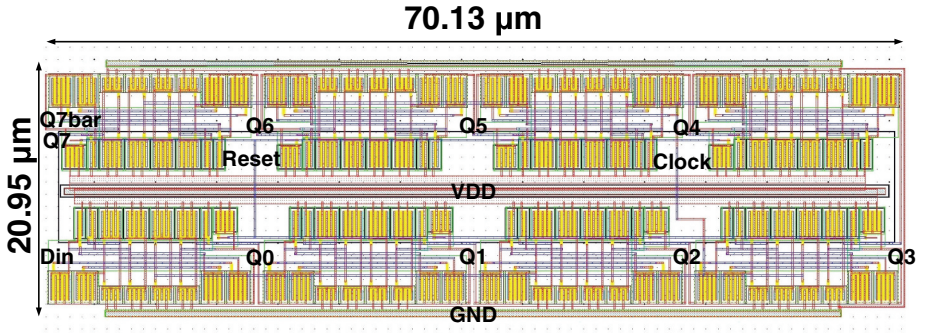

Figure 9. Proposed 8-bit DETFF-based shift register's core layout.

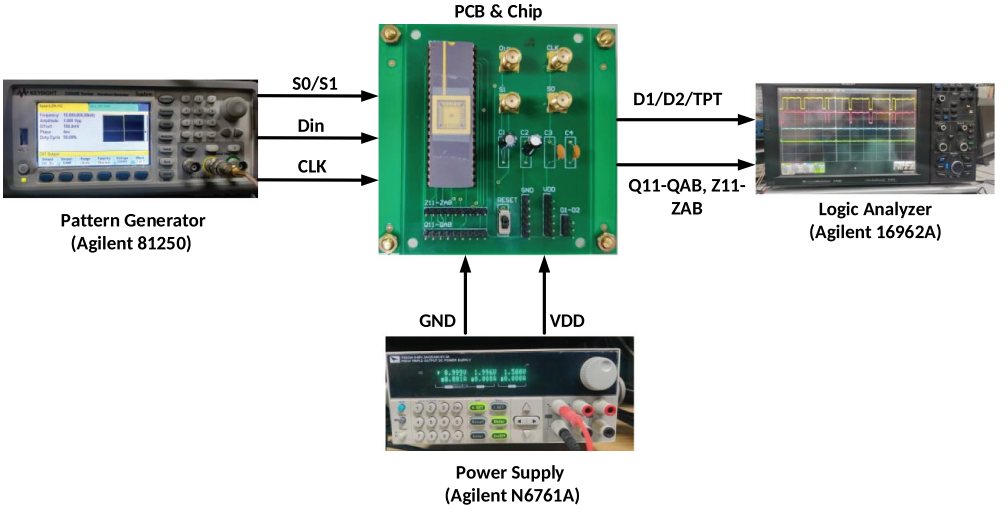

Figure 10. The chip's measurement setup.

Agilent 16962A monitored and observed the chip's functionality. The chip's functionality, power consumption, and time delay were tested and measured at a 25°C room temperature.

4. Measurement results and discussion

As shown in Figure 11, the chip's functionality is at its best at a maximum clock frequency of 200 MHz and supply voltage of 1.0 V. By contrast, the conventional shift register (Chu, 2019) fails at the same condition. The said chip was also tested and measured at 10% supply voltage variations to ensure the chip's robustness. At a clock frequency of 100 MHz, it is functioning correctly at varying supply voltages of 0.9 V, 1.0 V, and 1.1 V as shown in Figure 12, 13, and 14, respectively. At a 1-V supply and 100-MHz clock frequency, the power consumption is 3.352 mW, and the energy is 33.52 pJ.

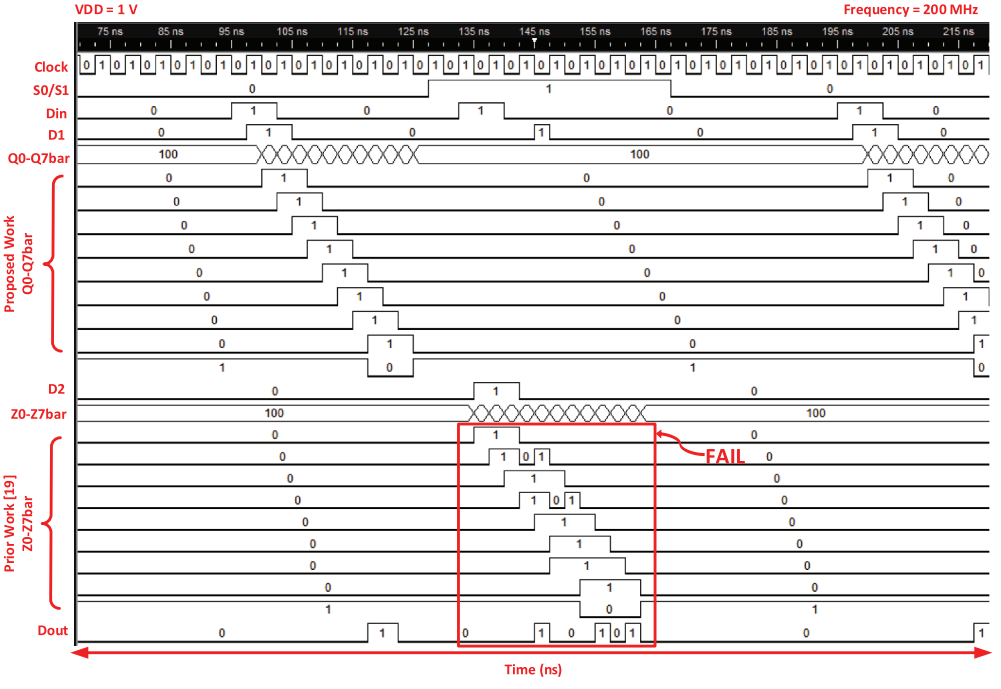

Figure 11. Chip measurement at a clock frequency of 200 MHz and supply voltage of 1.0 V.

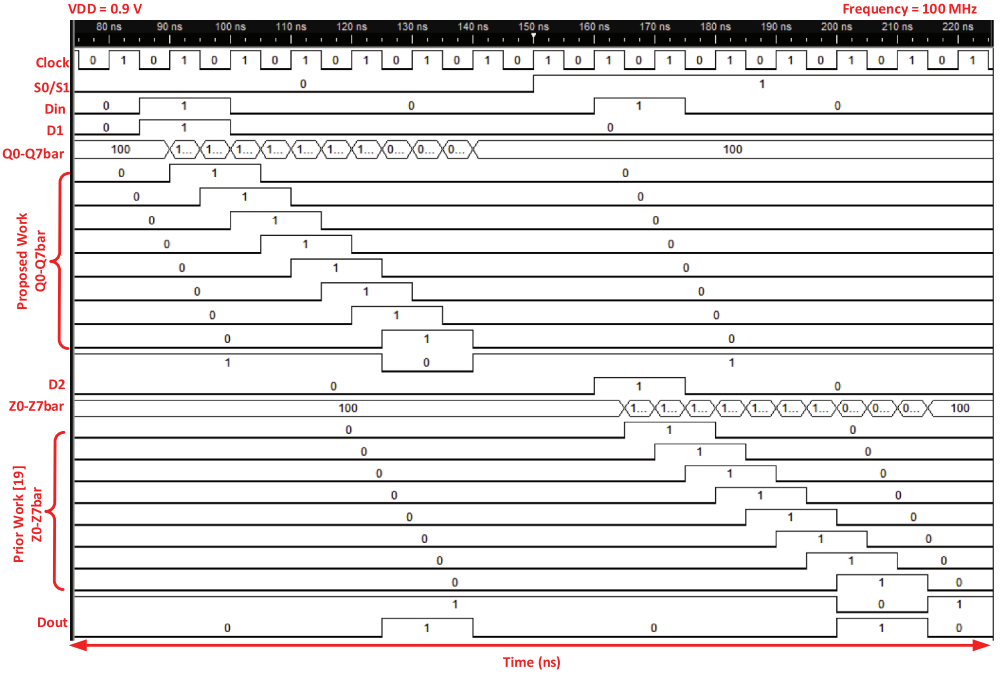

Figure 12. Chip measurement at a clock frequency of 100 MHz and supply voltage of 0.9 V.

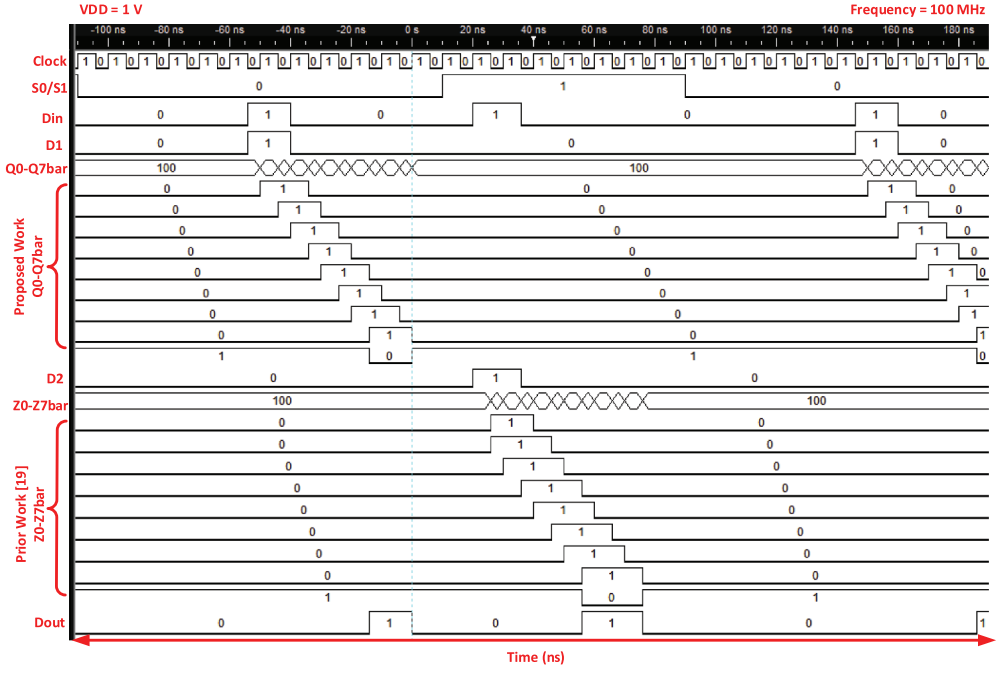

Figure 13. Chip measurement at a clock frequency of 100 MHz and supply voltage of 1.0 V.

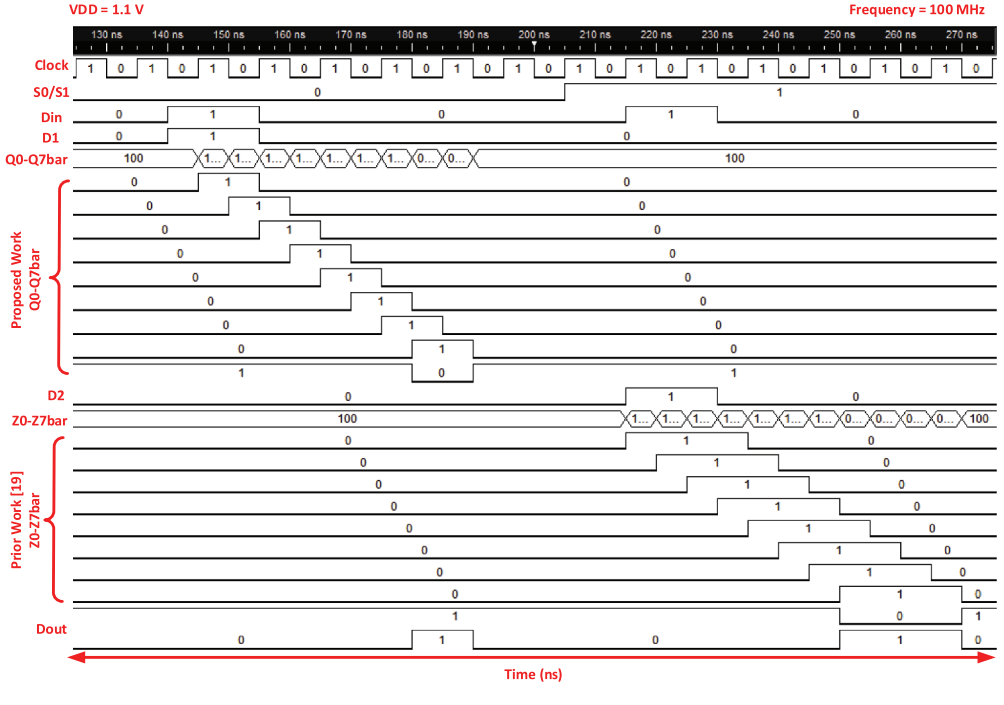

Figure 14. Chip measurement at a clock frequency of 100 MHz and supply voltage of 1.1 V.

Figure 15. Jitter measurement at a clock frequency of 1 MHz.

Figure 16. Jitter measurement at a clock frequency of 10 MHz.

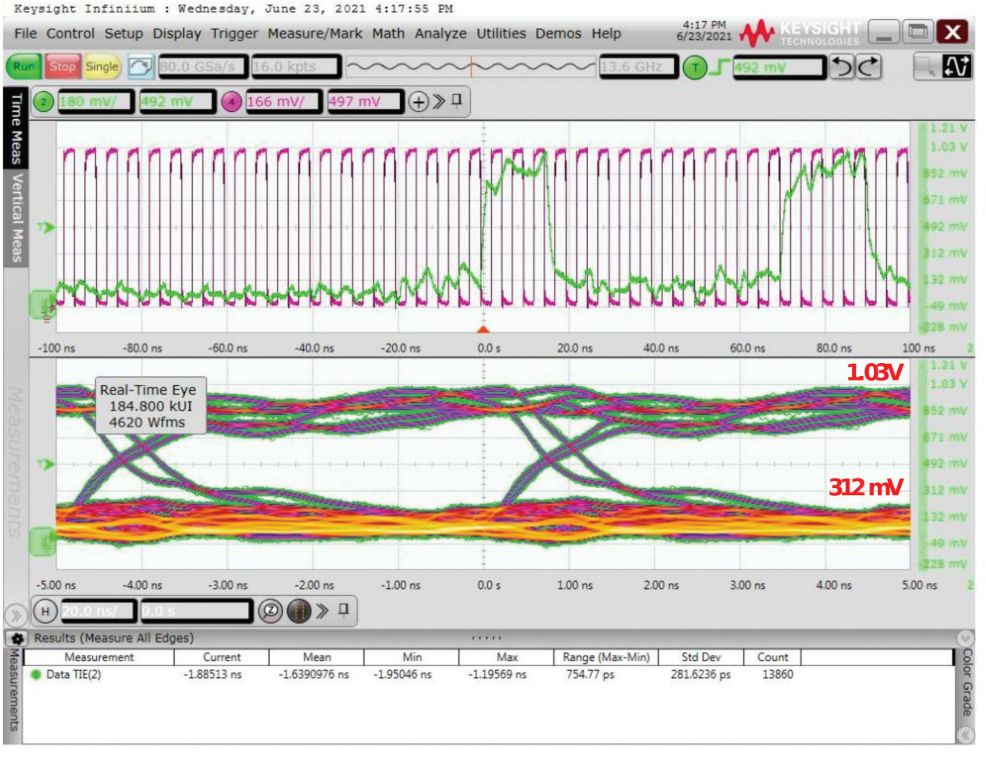

Figure 17. Jitter measurement at a clock frequency of 100 MHz.

Table 1. Jitter eye height and width at different frequencies.

Frequency (MHz)	Eye height (mV)	Eye width (ns)
1	942	400
10	942	48.3
100	427	4.58

Besides the functionality testing, jitter measurement was performed. Figure 15, 16, and 17 present the jitter eye diagram at 1 MHz, 10 MHz, and 100 MHz, respectively. Table 1 shows the jitter's eye width and height for the said frequencies, respectively. Notably, at a maximum frequency of 100 MHz, as shown in Figure 17, the jitter eye height and width are within the tolerable values, which are less than the supply voltage and pulse width, respectively.

The comparison of performance with different previous works related to DETFF are shown in Table 2. Since this study aims to develop a low-power, high-frequency, and long-bit length DETFF-based shift register, FOM (Figure of Merit) is proposed to determine which work has superior performance among all works, as shown in Equation (6). Moreover, Equation (7) shows the computation for the normalised power.

$$FOM = \frac{Power}{C_{Load} \times Frequency \times Bit\ Length} \tag{6}$$

Table 2. Comparison of Performance with Prior Works.

	ICCTICT[1]	ICISC[2]	WCSE[3]	IJCSIT[4]	ICISS[5]	Ours
Year	2016	2017	2018	2018	2019	2021
Process (nm)	180	180	180	180	180	90
Verification	Pre-sim	Pre-sim	Post-sim	Pre-sim	Pre-sim	Meas.
VDD (V)	1.8	N/A	1.8	1.8	N/A	1
Power (mW)	2.015	37.2	35.25	0.028	71	3.352
PDP (pJ)	1.154	86.4	78.18	0.0072	55	33.52
Delay (ns)	0.573	2.32	2.2	0.251	0.775	1.5
Frequency (MHz)	100	100	125	500	10	100
Bit length	4	8	8	1	8	8
Load (pF)	0.05	N/A	20	0.025	N/A	20
Norm. Power (mW)	0.621	N/A	10.86	0.00867	N/A	3.352
FOM	100.75	2.325	1.7625	2.24	44.375	**2.0937**

[1]Tyagi et al. (2016)
[2]Kumar et al. (2017)
[3]Baskoro et al. (2018)
[4]Yu and Tsai (2018)
[5]Bagalkoti et al. (2019)

$$Normalized\ Power = \frac{Power}{VDD^2} \tag{7}$$

According to Table 2, it can be seen that the DETFF based on Yu and Tsai (2018) has a smaller delay and higher operating frequency compared to our DETFF. Although our proposed DETFF-based shift register achieved the second best FOM among all works, our design is the only one proved on silicon and supplied with the lowest voltage of 1.0 V. Notably, prior works (Tyagi et al., 2016; Yu & Tsai, 2018) have smaller output load and shorter bit length resulting in their lower normalised power.

5. Conclusion

An 8-bit shift register featured with low-power DETFFs was developed using TSMC 90-nm CMOS technology. Though it has a longer delay and a lower operating frequency than prior DETFFs, it is the only one demonstrated and measured using prototype on silicon. It accommodated higher output capacitance load and longer bit length. Driven by a lower voltage of 1.0 V at a 100 MHz clock frequency, it has a power consumption of 3.352 mW, making it suitable for low-power applications. Lastly, as evidenced by the chip's functionality testing and jitter measurement, it has the best performance and operates at a maximum frequency of up to 200 MHz. Future works include implementing optimisation algorithms such as EHO in designing DETFFs.

Acknowledgments

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Disclosure statement

No potential conflict of interest was reported by the author(s).

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